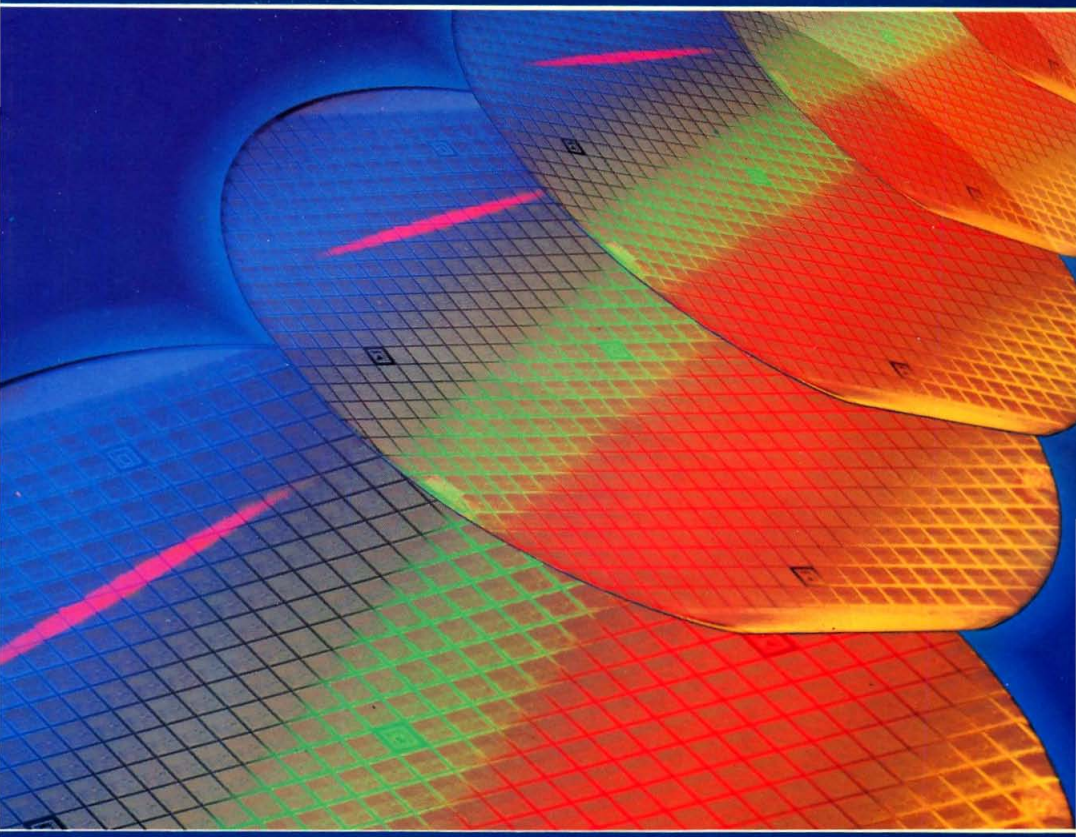
MILITARY & HI-REL DICE

DATA BOOK



THOMSON
COMPONENTS
SEMICONDUCTEURS

MILITARY & HI-REL DICE

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ALPHANUMERICAL INDEX

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INTRODUCTION

THOMSON SEMICONDUCTEURS Military and Space Division offers a large range of discretes, linear, microprocessor and memory products in die form. These dice are avalaible in a variety of quality classes.

SELECTION CLASSES

THOMSON SEMICONDUCTEUR Military and Space Division offers six selection classes:

E - 100% visual inspection low magnification
V - 100% visual inspection high magnification
N - Same as "V" + sampling lot with electrical testing
T - Same as "N" + burn-in
W -Same as "T" + life test 1000 hours
Z - Same as "W" + serialization

The selection criteria used for the "Z" level are according to those who are conditioned by the ESA.PSS-01-608 specification issue 2 "generic specification for hybrides microcircuits".

QUALITY ASSURANCE AND SCREENING PROCEDURE

(done according to THOMSON SEMICONDUCTEURS DMS SQ.32.S.0101 internal procedure except otherwise specified)

E	V	N	T	W	Z	
x	x	x	x	x	x	Wafer probe at room temperature
x	x	x	x	x	x	Wafer inspection
					x	SEM inspection - Scanning electron beam microscope
x	x	x	x	x	x	Sawing
x	x	x	x	x	x	Die visual inspection (100%) (1) E: low magnification,V, N, T, W, Z: high magnification
x	x	x	x	x	x	Die visual inspection (sampling) (1) LTPD = 5
		x	x	x	x	Sampling batch
		x	x	x	x	Assembly (55 parts standard)
		x	x	x	x	Precap inspection 100% (1)
		x	x	x	x	Bond pull test (sampling) (2) IC's: LTPD = 10 Discretes: 4 parts, all wires, no reject allowed (*)
		x	x	x	x	Die shear test (sampling) (3) 3 parts no reject allowed (*)
		x	x	x	x	Sealing
					x	Serialization
		x	x	x	x	Electrical measurement (4) + 25°C, Tmax, Tmin (as applicable) 2 rejects allowed(*)
			x	x	x	Burn in N, T, W: 160 h - Z: 240 h — 3 rejects allowed (*)
			x	x	x	Electrical measurement + 25°C
					x	Drift calculation
				x	x	Electrical measurement + 25°C (4) (*) 2 rejects allowed (*)
		x	x	x	x	Test report
x	x	x	x	x	x	Final acceptance

(1) IC'S: V, N, T, W: MIL-STD-883C Method 2010 Cond B
Z: MIL-STD-883C Method 2010 Cond A
DISCRETES: E, V, N, T W: MIL-STD-750 Method 2072 or 2073 (as applicable)
Z: ESA/SCC 20400

(2) MIL-STD-883 Method 2011

(3) MIL-STD-883 Method 2019

(4) Electrical measurement N, T, W: go-no go
Z: read and record

(*) Standard level

QUALIFICATION LOT

To better qualify the dice, THOMSON SEMICONDUCTEURS DMS offers to qualify fully assembled parts coming from the same diffusion lot.

The sample quantity required for the qualification lot is in accordance to the statistical guarantee brought by this lot. The array below indicates the qualification lot size and the acceptance or reject conditions for each test.

TESTS	QUALITY LEVEL	SIZE 1 (1)	SIZE 2 (2)	SIZE 3 (standard)
Electrical (*) test at: 3 temperatures for IC's (25°C for discretes)	N, T, W, Z	23 pcs, 0 reject allowed LTPD better than 10	38 pcs 1 reject allowed LTPD = 10	55 pcs 2 rejects allowed LTPD better than 10
Electrical test after burn-in at 25°C	T, W, Z	23 pcs 1 reject allowed LTPD better than 15	37 pcs 2 rejects allowed LTPD better than 15	53 pcs 3 rejects allowed LTPD better than 15
Electrical test after life test at 25°C	W, Z	22 pcs 0 reject allowed LTPD = 10	35 pcs 1 reject allowed LTPD better than 10	50 pcs 2 rejects allowed LTPD better than 10

The packages used for the above tests are those indicated on the respective data sheet.

The sample sizes to be tested are the minimum to assure, with a 90% confidence, that a lot having percent defective equal to the specified LTPD will not be accepted (single sample). Sample sizes are based upon the Poisson exponential binomial limit.

LTPD = Lot Tolerance Percentage Defect

(1) : By special request only
(2) : ESA PSS.01.608 specification
(*) : done in accordance with the packaged product data sheet.

PRODUCT SPECIFICATIONS

For each die the following information is indicated in the data sheet:

MECHANICAL INFORMATION:

- pad layout
- pad size
- die size
- die thickness
- metallization
- passivation

ELECTRICAL INFORMATION

- maximum ratings
- electrical parameters at 25°C
- die back side bias if applicable

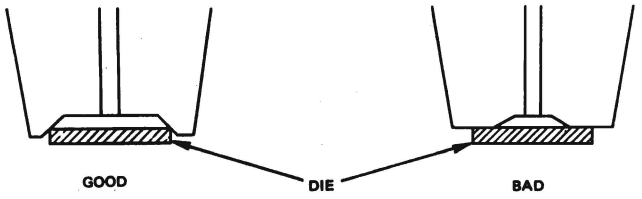
DOCUMENTATION

All die shipments from THOMSON SEMICONDUCTEURS DMS are bundled with the following documentation:

Die lot: Certificate of compliance (COC)
Qualification lot (level N, T, W, Z):
- certificate of compliance,
- test report (N, T, W)
- test data for each individual serialized part (Z).

DIE HANDLING CAUTIONS

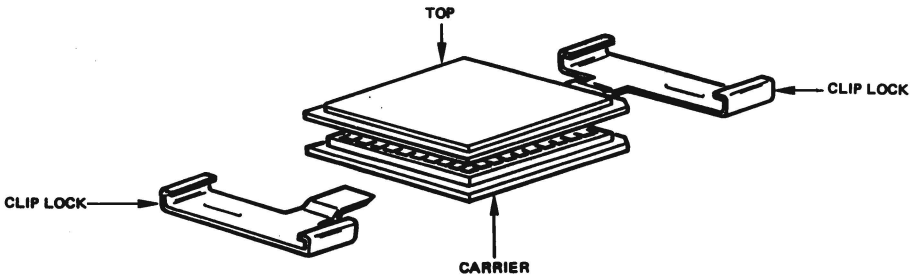
Special care is required in handling dice.
We recommend to pick the dice up by using transfer pipette adapted to the die sizes, to prevent any damage, as scratching the surface of the dice.



All handling tools and workstations must be protected against all pollution and electrical static discharge (ESD).

PACKAGING

Shipment are delivered in properly sized waffle packs.
The waffle packs use antistatic and dust free materials and are closed using special clip locks preventing undue opening.
They are inserted in vacuum packed plastic bag.
Waffle packs must be opened for inspection by qualified personnel only.

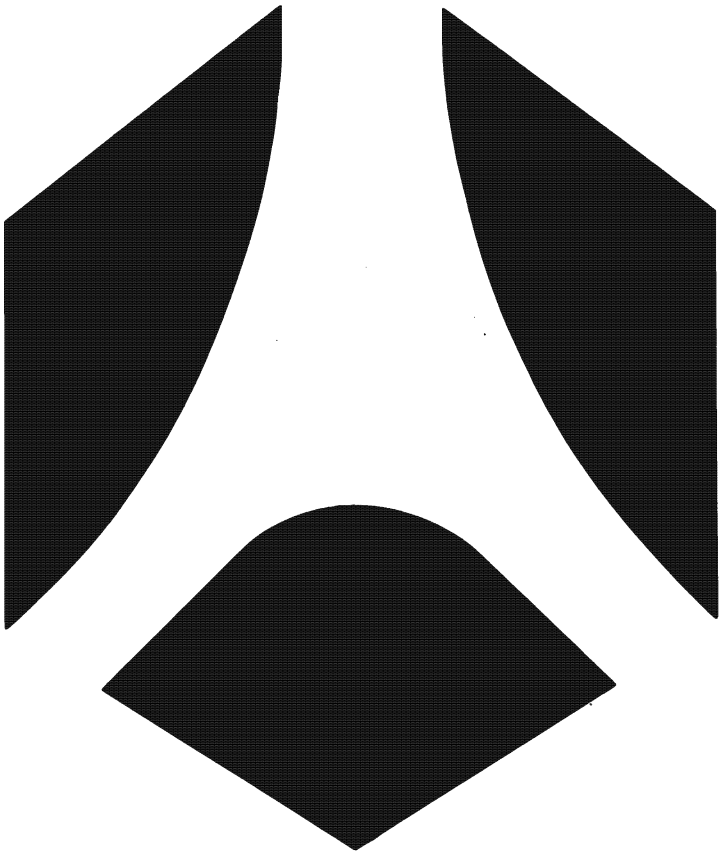


The content of each box is identified by a THOMSON SEMICONDUCTEURS sticker indicating:

- product type,
- lot number,
- quantity,
- date of shipment,
- quality control approval.

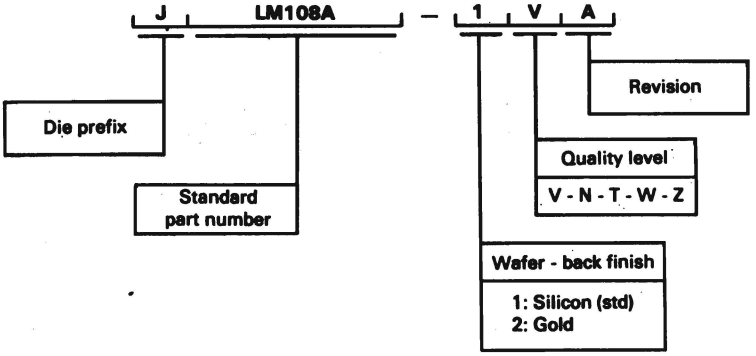
ORDERING INFORMATION

All dice should be ordered with the THOMSON SEMICONDUCTEUR DMS identification code, including a revision issue except otherwise specified, in accordance with the respective data *sheet. See chapter* heads for details.



Operational amplifiers

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J LF155		X					X	X	A
J LF156		X	X	X	X	X	X	X	A
J LF157		X					X	X	A
J LF355		X					X	X	A
J LF356		X	X	X	X	X	X	X	A
J LF357		X					X	X	A
J LM101A		X	X	X	X	X	X	X	A
J LM301A		X	X	X			X	X	A
J LM108		X	X	X	X	X	X	X	A
J LM108A		X	X	X	X	X	X	X	A
J LM308		X	X	X			X	X	A
J LM308A		X	X	X			X	X	A
J LM124		X	X	X	X	X		X	A
J LM324		X	X	X				X	A
J LM146		X						X	A
J LM346		X						X	A
J LM14B		X	X	X	X	X		X	A
J LM348		X	X	X				X	A
J LM158		X	X	X	X	X	X	X	A
J LM358		X	X	X			X	X	A
J LM1458		X	X	X			X	X	A
J LM1558		X	X	X	X	X	X	X	A
J TL061		X	X	X	X	X	X	X	A
J TL062		X	X	X	X	X	X	X	A
J TL064		X	X	X	X	X		X	A
J TL071		X					X	X	A
J TL072		X	X	X	X	X	X	X	A
J TL074		X	X	X	X	X		X	A
J TL081		X					X	X	A
J TL082		X	X	X	X	X	X	X	A
J TL084		X	X	X	X	X		X	A
J UA741		X	X	X	X	X	X	X	A
J UA776		X	X	X	X	X	X	X	A

THOMSON COMPONENTS SEMICONDUCTEURS

J LF155/355 • J LF156/356 • J LF157/357

J-FET INPUT SINGLE OPERATIONAL AMPLIFIER

These circuits are monolithic J-FET input operational amplifiers incorporating well matched high voltage J-FETs on the same chip with standard bipolar transistors.

These amplifiers feature low input bias currents, low input offset voltage and input offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection.

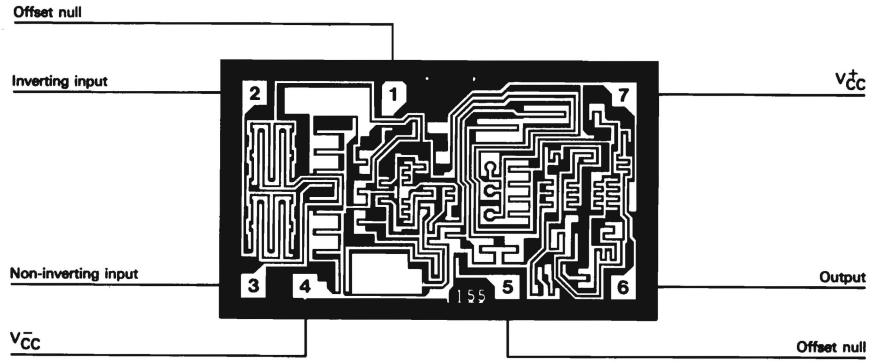
The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low I/f noise corner.

- Precision high speed integrators.
- Fast D/A and A/D converters.
- High impedance buffers.
- Wideband, low noise, low drift amplifiers.
- Logarithmic amplifiers.
- Photocell amplifiers.
- Sample and hold circuits.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P858
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 2.00 x 1.20mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	J LF355 J LF356 J LF357	J LF155 J LF156 J LF157	Unit
Supply voltage	V_{CC}	±18	±22	V
Differential input voltage	V_{ID}	±30	±40	V
Input voltage - (Note 1)	V_I	±16	±20	V
Operating free-air temperature range	T_{oper}	0 to + 70	−55 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ±15 V (Unless otherwise specified)

Characteristic	Symbol	J LF155, J LF156, J LF157			J LF355, J LF356, J LF357			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	3	5	–	3	10	mV
Input offset current	I_{IO}	–	3	–	–	3	–	pA
Input bias current	I_{IB}	–	30	–	–	30	–	pA
Large signal voltage gain (V_{OPP} = ±10 V, R_L = 2 kΩ)	A_{VD}	50	200	–	25	200	–	V/mV
Supply voltage rejection ratio - (Note 2)	SVR	86	100	–	86	100	–	dB
Supply current J LF155, J LF355 J LF156, J LF356 J LF157, J LF357	I_{CC}	 – – –	 2 5 5	 4 7 7	 – – –	 2 5 5	 4 10 10	mA
Input voltage range	V_I	±11	+15.1 −12	–	±11	+15.1 −12	–	V
Common-mode rejection ratio	CMR	86	100	–	86	100	–	dB
Output voltage swing R_L = 10 kΩ R_L = 2 kΩ	V_{OPP}	 ±12 ±10	 ±13 ±12	 – –	 ±12 ±10	 ±13 ±12	 – –	V
Gain-bandwidth product J LF155, J LF355 J LF156, J LF356 J LF157, J LF357	GB_p	 1.5 3.5 16	 2.5 5 20	 – – –	 1.5 3.5 16	 2.5 5 20	 – – –	MHz
Slew rate A_V = 1 J LF155, J LF355 J LF156, J LF356 A_V = 5 J LF157, J LF357	S_{VO}	 – – –	 5 12 50	 – – –	 – – –	 5 12 50	 – – –	V/μs

NOTES :

1- Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

2- Supply voltage rejection is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.DSJLF1556735567

THOMSON COMPONENTS SEMICONDUCTEURS

J LM101A • J LM301A

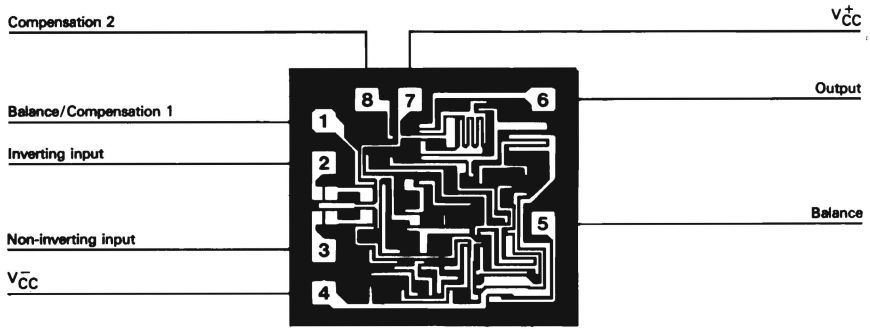
SINGLE OPERATIONAL AMPLIFIER

The LM101A is a general-purpose operational amplifier. This amplifier offers many features : supply voltages from ± 5 V to ± 20 V, low current drain, overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitors. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application : slew rates of 10 V/μs and bandwidths of 3.5 MHz can be easily achieved. In addition, the circuit can be used as a comparator with differential inputs up to ± 30 V. The output can be clamped at any desired level to make it compatible with logic circuits.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P850
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.20 x 1.30mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-.

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MAXIMUM RATINGS

Rating	Symbol	LM101A	LM301A	Unit
Supply voltage	V_{CC}	±22	±18	V
Differential input voltage	V_{ID}	±30	±30	V
Input voltage	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C,
J LM101A : ±5 V ≤ V_{CC} ≤ ±20 V, C1 = 30 pF
J LM301A : ±5 V ≤ V_{CC} ≤ ±15 V, C1 = 30 pF
(Unless otherwise specified)

Characteristic	Symbol	J LM101A			J LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	0.7	2	–	2	7.5	mV
Input offset current	I_{IO}	–	1.5	10	–	3	50	nA
Input bias current	I_{IB}	–	30	75	–	70	250	nA
Large signal voltage gain (V_{CC} = ±15 V, R_L = 2 kΩ, V_O = ±10 V)	A_{VD}	50	160	–	25	160	–	V/mV
Supply voltage rejection ratio (R_S = 50 kΩ)	SVR	80	96	–	70	96	–	dB
Supply current (V_{CC} = +15 V)	I_{CC}^+, I_{CC}^-	–	1.8	3	–	1.8	3	mA
Input voltage range (V_{CC} = $V_{CC(max)}$)	V_I	±15	–	–	±12	–	–	V
Common-mode rejection ratio (R_S ≤ 50 kΩ)	CMR	80	96	–	70	90	–	dB
Output voltage swing (V_{CC} = ±15 V) R_L = 2 kΩ R_L = 10 kΩ	V_{OPP}	 ±10 ±12	 ±13 ±14	 – –	 ±10 ±12	 ±13 ±14	 – –	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.:DS/LM101A/LM301A

THOMSON COMPONENTS SEMICONDUCTEURS

J LM108/308 • J LM108A/308A

PRECISION SINGLE OPERATIONAL AMPLIFIER

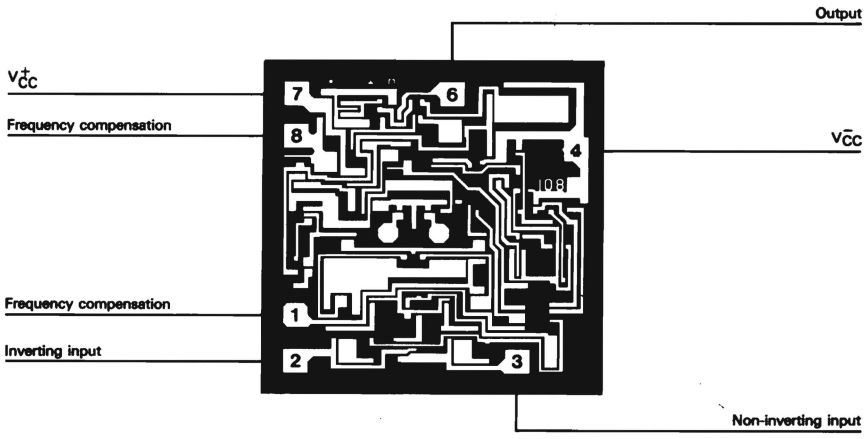
The LM108,A is a precision operational amplifier having specifications a factor ten better than FET amplifiers over a −55°C to +125°C temperature range. Selected units are available with offset voltages less than 1 mV and drifts less than 5μV/°C. This makes it possible to eliminate offset adjustments, in most cases.

The device operates with supply voltages from ±2 V to ±20 V (LM308 : ±2 V to ±15 V) and has sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P126
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.56 x 1.56mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^{-}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	J LM108,A	LM308,A	Unit
Supply voltage	V_{CC}	± 20	± 18	V
Input voltage - (Note 2)	V_I	± 15	± 15	V
Input offset current - (Note 1)	I_{IO}	± 10	± 10	mA
Operating free-air temperature range	T_{oper}	− 55 to + 125	0 to + 70	°C
Storage temperature range	T_{stg}	− 65 to + 150	− 55 to + 125	°C

NOTES :

1 – The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

2 – For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, (Unless otherwise specified)
J LM108A : ± 5 V ≤ V_{CC} ≤ ± 20 V
J LM308A : ± 5 V ≤ V_{CC} ≤ ± 15 V

Characteristic	Symbol	J LM108A			J LM308A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	V_{IO}	–	0.3	0.5	–	0.3	0.5	mV
Input offset current	I_{IO}	–	0.05	0.2	–	0.2	1	nA
Input bias current	I_{IB}	–	0.8	2	–	1.5	7	nA
Large signal voltage gain (V_{CC} = ± 15 V, R_L ≥ 10 kΩ, V_O = ± 10 V)	A_{VD}	80	300	–	80	300	–	V/mV
Supply voltage rejection ratio	SVR	96	110	–	96	110	–	dB
Supply current	I_{CC}^+, I_{CC}^-	–	0.3	0.6	–	0.3	0.8	mA
Input voltage range (V_{CC} = ± 15 V)	V_I	± 13.5	–	–	± 14	–	–	V
Common-mode rejection ratio	CMR	96	110	–	96	110	–	dB
Output voltage swing (V_{CC} = ± 15 V, R_L = 10 kΩ)	V_{OPP}	± 13	± 14	–	± 13	± 14	–	V

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, (Unless otherwise specified)
J LM108 : ± 5 V ≤ V_{CC} ≤ ± 20 V
J LM308 : ± 5 V ≤ V_{CC} ≤ ± 15 V

Characteristic	Symbol	J LM108			J LM308			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	V_{IO}	–	0.7	2	–	2	7.5	mV
Input offset current	I_{IO}	–	0.05	0.2	–	0.2	1	nA
Input bias current	I_{IB}	–	0.8	2	–	1.5	7	nA
Large signal voltage gain (V_{CC} = ± 15 V, R_L ≥ 10 kΩ, V_O = ± 10 V)	A_{VD}	50	300	–	25	300	–	V/mV
Supply voltage rejection ratio	SVR	80	96	–	80	96	–	dB
Supply current	I_{CC}^+, I_{CC}^-	–	0.3	0.6	–	0.3	0.8	mA
Input voltage range (V_{CC} = ± 15 V)	V_I	± 13.5	–	–	± 14	–	–	V
Common-mode rejection ratio	CMR	85	100	–	80	100	–	dB
Output voltage swing (V_{CC} = ± 15 V, R_L = 10 kΩ)	V_{OPP}	± 13	± 14	–	± 13	± 14	–	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.:DSJLM108308A

THOMSON COMPONENTS SEMICONDUCTEURS

J LM124 • J LM324

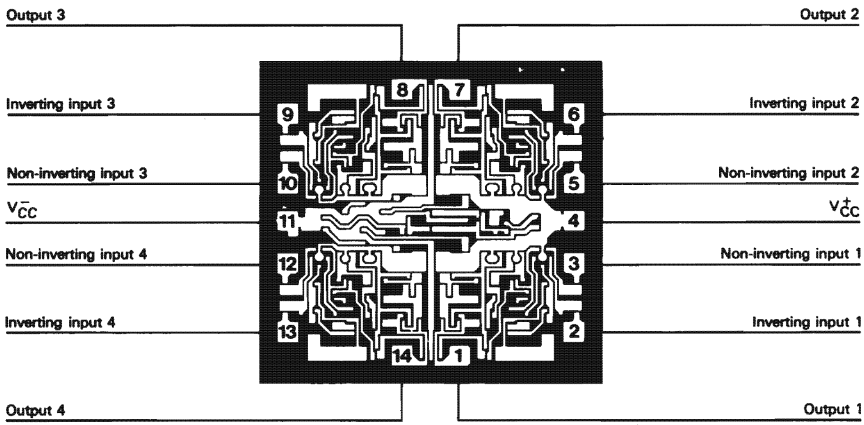
LOW POWER QUAD OPERATIONAL AMPLIFIER

This circuit consists of four independant high gain, internally frequency compensated operational amplifiers which as designed specifically for automotive and industrial control systems. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P876
PAD SIZE	: 0.10 x 0.10mm
DIE SIZE	: 1.53 x 1.59mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: TO116 (Ceramic)



Back side bias : V_{CC}^-

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	J LM124	J LM324	Unit
Supply voltage	V_{CC}	±16 or 32	±16 or 32	V
Differential input voltage	V_{ID}	32	32	V
Input voltage	V_I	−0.3 to +32	−0.3 to +32	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC}^+ = +5$ V, $V_{CC}^- = GND$
(Unless otherwise specified)

Characteristic	Symbol	J LM124			J LM324			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S = 0\ \Omega$) - Note 1	V_{IO}	–	2	5	–	2	7	mV
Input offset current	I_{IO}	–	3	30	–	5	50	nA
Input bias current - (Note 2)	I_{IB}	–	45	100	–	45	250	nA
Large signal voltage gain ($V_{CC} = \pm 15$ V, $R_L = 2$ kΩ)	A_{VD}	50	100	–	25	100	–	V/mV
Supply voltage rejection ratio	SVR	65	100	–	65	100	–	dB
Supply current ($R_L = \infty$ for all amplifiers) $V_{CC} = +5$ V $V_{CC} = +30$ V	I_{CC}^+, I_{CC}^-	 – –	 0.7 1.5	 1.2 3	 – –	 0.8 1.5	 1.2 3	mA
Input voltage range ($V_{CC}^+ = +30$ V) - Note 3	V_I	0	–	$V_{CC}^+ - 1.5$	0	–	$V_{CC}^+ - 1.5$	V
Common-mode rejection ratio	CMR	70	85	–	65	70	–	dB
Output short-circuit current	I_{OS}	–	40	60	–	40	60	mA
Output current ($V_{CC}^+ = +15$ V, $V_I^+ = +1$ V, $V_I^- = 0$ V)	I_O	20	40	–	20	40	–	mA
Output current sink ($V_I^+ = 0$ V, $V_I^- = +1$ V) $V_{CC}^+ = +15$ V $V_O = +200$ mV	$I_{O(sink)}$	 10 0.012	 20 0.05	 – –	 10 0.012	 20 0.05	 – –	mA
Output voltage swing ($V_{CC}^+ = +5$ V, $R_L \geq 2$ kΩ)	V_{OPP}	0	–	$V_{CC}^+ - 1.5$	0	–	$V_{CC}^+ - 1.5$	V
High level output voltage ($V_{CC}^+ = +30$ V, $R_L = 2$ kΩ)	V_{OH}	26	–	–	26	–	–	V
Low level output voltage ($R_L \leq 10$ kΩ)	V_{OL}	–	5	20	–	5	20	mV

NOTES :

1 – $V_O = +1.4$ V, $R_S = 0\ \Omega$, $+5\ V \leq V_{CC}^+ \leq +30$ V, $V_{CC}^- =$ Ground, $0 \leq V_I \leq (V_{CC}^+ - 1.5\ V)$

2 – The direction of the output current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

3 – The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5$ V, but either or both inputs can go to +32 V without damage.

Ref.DSJLM124JLM324

THOMSON COMPONENTS SEMICONDUCTEURS

J LM146 • J LM346

PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The LM346 consists of four independent, high gain, internally compensated, low power programmable amplifiers. Two external resistors (R_{set}) allow the user to program the gain-bandwith product, slew rate, supply current, input bias current, input offset current and input noise. For example the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way other amplifier characteristics can be tailored to the application.

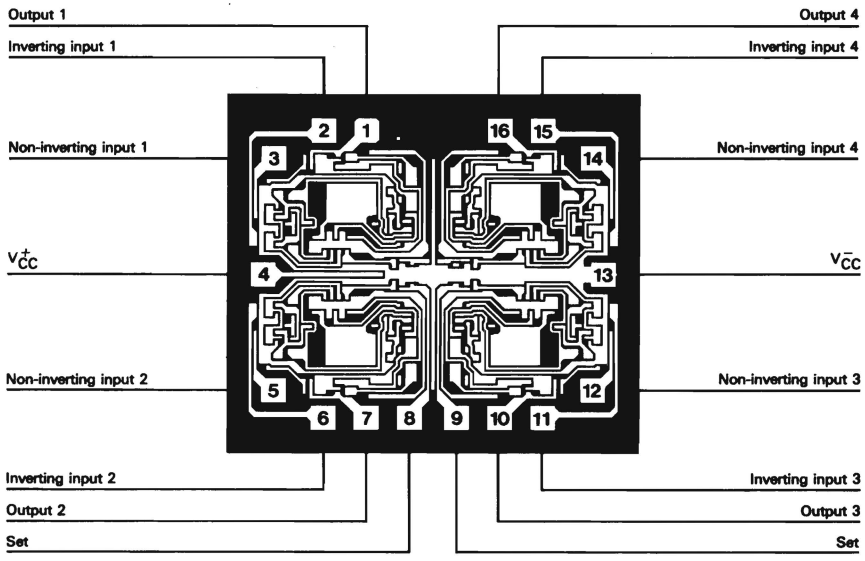
PROGRAMMING EQUATIONS :
Total supply current = 1.4 mA (I_{set} = 10 µA)
Gain-bandwith product = 1 MHz (I_{set} = 10 µA)
Slew rate = 0.4 V/µs (I_{set} = 10 µA)
Input bias current ≃ 50 nA (I_{set} = 10 µA)
I_{set} = current into terminals 8 and 9

$$I_{set} = \frac{V_{CC}^{+} - V_{CC}^{-} - 0.6V}{R_{set}}$$

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	XO43
PAD SIZE	:	0.12 x 0.12mm
DIE SIZE	:	1.88 x 1.67mm
DIE THICKNESS	:	0.375mm ± 0.025
METALLIZATION	:	Al (front side)
PASSIVATION	:	Nitride
REVISION	:	A
QUALIFICATION		
LOT CASE	:	DIL 16 pins (Ceramic)



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J LM146	J LM346	Unit
Supply voltage	V_{CC}	±22	±18	V
Input voltage - (Note 1)	V_I	±15	±15	V
Differential input voltage	V_{ID}	±30	±30	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

NOTE : 1 − For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ± 15 V, I_{set} = 10 µA, (Unless otherwise specified)

Characteristic	Symbol	J LM146			J LM346			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 50\ \Omega$)	V_{IO}	—	0.5	5	—	0.5	6	mV
Input offset current	I_{IO}	—	2	20	—	2	100	nA
Input bias current	I_{IB}	—	50	100	—	50	250	nA
Large signal voltage gain ($\Delta V_O = \pm 10$ V, $R_L = 10$ kΩ)	A_{VD}	100	1000	—	50	1000	—	V/mV
Supply voltage rejection ratio ($R_S \leq 10$ kΩ)	SVR	80	100	—	74	100	—	dB
Supply current	I_{CC}	—	1.4	2	—	1.4	2.5	mA
Input voltage range	V_I	±13.5	±14	—	±13.5	±14	—	V
Common-mode rejection ratio ($R_S \leq 10$ kΩ)	CMR	80	100	—	70	100	—	dB
Output short-circuit current	I_{OS}	5	20	30	5	20	30	mA
Output voltage swing ($R_L \geq 10$ kΩ)	V_{OPP}	±12	±14	—	±12	±14	—	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJLM146JLM346

THOMSON COMPONENTS SEMICONDUCTEURS

J LM148 • J LM348

DIFFERENTIAL INPUT QUAD OPERATIONAL AMPLIFIER

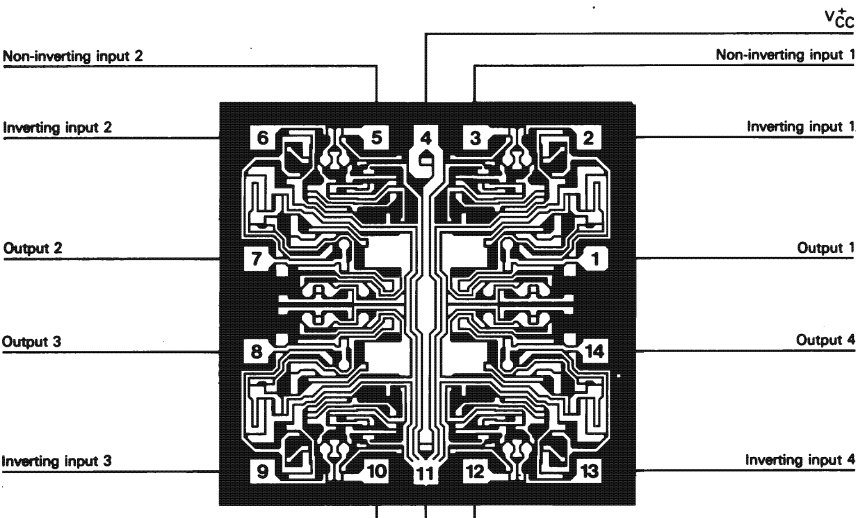
The LM148 consists of four independent, high gain internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar UA741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single UA741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard UA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple UA741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P950
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.90 x 1.88mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-2 Ceramic) TO116



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J LM148	J LM348	Unit
Supply voltage	V_{CC}	±22	±18	V
Differential input voltage	V_{ID}	±44	±36	V
Input voltage	V_I	±22	±18	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ±15 V, (Unless otherwise specified)

Characteristic	Symbol	J LM148			J LM348			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1	5	–	1	6	mV
Input offset current	I_{IO}	–	4	25	–	4	50	nA
Input bias current	I_{IB}	–	30	100	–	30	200	nA
Large signal voltage gain (V_O = ±10 V, $R_L \geq 2$ kΩ)	A_{VD}	50	160	–	25	160	–	V/mV
Supply current (4 amplifiers)	I_{CC}	–	2.4	3.6	–	2.4	4.5	mA
Input voltage range	V_I	±12	–	–	±12	–	–	V
Supply voltage rejection ratio ($R_S \leq 10$ kΩ)	SVR	77	96	–	77	96	–	dB
Common-mode rejection ratio ($R_S \leq 10$ kΩ)	CMR	70	90	–	70	90	–	dB
Output voltage swing R_L = 2 kΩ R_L = 10 kΩ	V_{OPP}	 ±10 ±12	 ±12 ±13	 – –	 ±10 ±12	 ±12 ±13	 – –	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJLM148JLM348

THOMSON COMPONENTS SEMICONDUCTEURS

J LM158 • J LM358

LOW POWER DUAL OPERATIONAL AMPLIFIER

This circuit consists of two independent, high gain, internally frequency compensated amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, this circuit can be directly operated off the standard + 5V power supply voltage which is used in logic systems and will easily provides the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground, and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

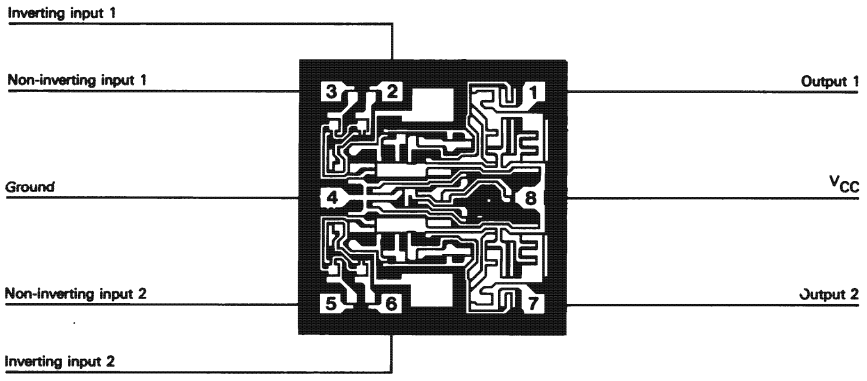
The gain-bandwidth product is temperature compensated.

The input bias current is temperature compensated.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P880
PAD SIZE	: 0.10 x 0.10mm
DIE SIZE	: 1.27 x 1.21mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	J LM158	J LM358	Unit
Supply voltage	V_{CC}	+32	+32	V
Differential input voltage	V_{ID}	+32	+32	V
Input voltage	V_i	−0.3 to +32	−0.3 to +32	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5 V, (Unless otherwise specified)

Characteristic	Symbol	J LM158			J LM358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage - Note 1	V_{IO}	–	±2	±5	–	±2	±7	mV
Input offset current	I_{IO}	–	±3	±30	–	±5	±50	nA
Input bias current - Note 2	I_{IB}^+, I_{IB}^-	–	45	150	–	45	250	nA
Large signal voltage gain (V_{CC} = +15 V, $R_L \geq 2$ kΩ)	A_{VD}	50	100	–	25	100	–	V/mV
Supply voltage rejection ratio	SVR	65	100	–	65	100	–	dB
Supply current ($R_L = \infty$)	I_{CC}	–	0.7	1.2	–	0.7	1.2	mA
Input voltage range (V_{CC} = +30 V) - Note 3	V_I	0	–	V_{CC}-1.5	0	–	V_{CC}-1.5	V
Common-mode rejection ratio	CMR	70	85	–	65	70	–	dB
Output current (V_{CC} = +15 V. V_I^+ = +1 V, V_I^- = 0 V)	I_O	20	40	–	20	40	–	mA
Output current sink (V_I^- = −1 V, V_I^+ = 0 V) V_{CC} = +15 V V_O = +0.2 V	$I_{O(sink)}$	 10 12	 20 50	 – –	 10 12	 20 50	 – –	 mA µA
Output voltage swing (R_L = 2 kΩ)	V_{OPP}	0	–	V_{CC}-1.5	0	–	V_{CC}-1.5	V

NOTES :

1 – $V_O \approx 1.4$ V, R_S = 0, +5 V ≤ V_{CC} ≤ +30 V, 0 ≤ V_I ≤ V_{CC} − 1,5 V

2 – The direction of the input current is out of the chip. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

3 – The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1.5 V. But either or both inputs can go to +32 V without damage.

Printed in France

Ref.DS-JLM158JLM358

THOMSON COMPONENTS SEMICONDUCTEURS

J LM1458 • J LM1558

DUAL OPERATIONAL AMPLIFIER

The LM1458 and LM1558 are high performance monolithic dual operational amplifiers constructed on a single silicon chip. They are intended for a wide range of analog applications.

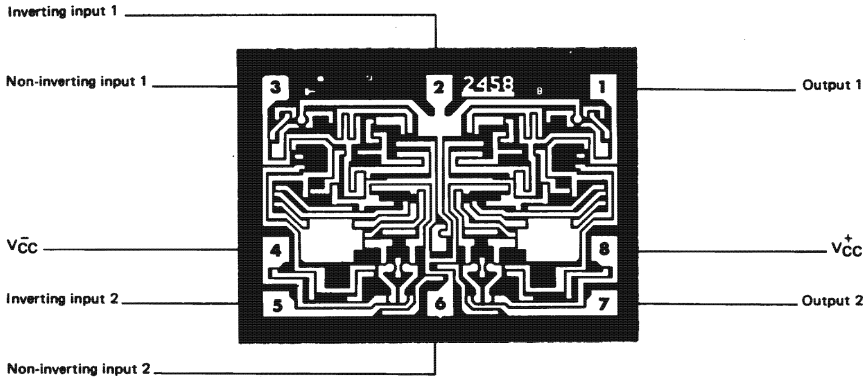
- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feed back applications. The internal compensation network (6 dB/octave) insures stability in closed loop applications.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P303
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 1.12 x 1.52mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage J LM1458 J LM1558	V_{CC}	 ±18 ±22	V
Input voltage	V_I	±15	V
Differential input voltage	V_{ID}	±30	V
Operating free-air temperature range J LM1558 J LM1458	T_{oper}	 −55 to +125 0 to + 70	°C
Storage temperature range J LM1558 J LM1458	T_{stg}	 −65 to +150 −55 to +125	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ±15 V, (Unless otherwise specified)

Characteristic	Symbol	J LM1558			J LM1458			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 10$ kΩ)	V_{IO}	—	1	5	—	1	6	V
Input offset current	I_{IO}	—	20	200	—	20	200	nA
Input bias current	I_{IB}	—	80	500	—	80	500	nA
Large signal voltage gain (V_O = ±10 V, $R_L \geq 2$ kΩ)	A_{VD}	50	200	—	20	200	—	V/mV
Supply voltage rejection ratio ($R_S \leq 10$ kΩ)	SVR	—	30	150	—	30	150	μV/V
Supply current	I_{CC}^+, I_{CC}^-	—	2.3	5	—	2.3	5.6	mA
Input voltage range	V_I	±12	±13	—	±12	±13	—	V
Common-mode rejection ratio ($R_S \leq 10$ kΩ)	CMR	70	90	—	70	90	—	dB
Output voltage swing $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	V_{OPP}	 ±12 ±10	 ±14 ±13	 — —	 ±12 ±10	 ±14 ±13	 — —	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/LM1458/LM1558

THOMSON COMPONENTS SEMICONDUCTEURS

J TL061

LOW POWER J-FET INPUT SINGLE OPERATIONAL AMPLIFIER

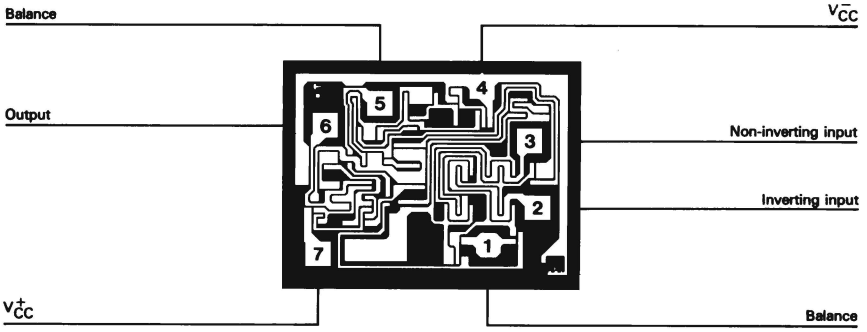
The TL061 is low power J-FET input single operational amplifier. This J-FET input operational amplifier incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P884
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.35 x 1.05mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J TL061M	J TL061C	Unit
Supply voltage - (Note 1)	V_{CC}	±18	±18	V
Differential input voltage - (Note 2)	V_{ID}	±30	±30	V
Input voltage - (Note 3)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES :

1 – All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^{+} and V_{CC}^{-}.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ± 15 V, (Unless otherwise specified)
All characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL061M			J TL061C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	3	6	–	5	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	nA
Input bias current*	I_{IB}	–	30	–	–	30	–	nA
Input common-mode voltage range	V_I	±11	±12	–	±10	±11	–	V
Output voltage swing (R_L = 10 kΩ)	V_{OPP}	20	27	–	20	27	–	V
Large signal voltage gain ($R_L \geqslant$ 10 kΩ, V_O = ± 10 V)	A_{VD}	4	6	–	3	6	–	V/mV
Small signal bandwidth (R_L = 10 kΩ)	GW_R	0.7	1	–	0.7	1	–	MHz
Common-mode rejection ratio ($R_S \leqslant$ 10 kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$, $R_S \leqslant$ 10 kΩ)	SVR	80	95	–	70	95	–	dB
Supply current (no load, no signal)	I_{CC}	–	200	250	–	200	250	μA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/JTL061

THOMSON COMPONENTS SEMICONDUCTEURS

J TL062

LOW POWER J-FET INPUT DUAL OPERATIONAL AMPLIFIER

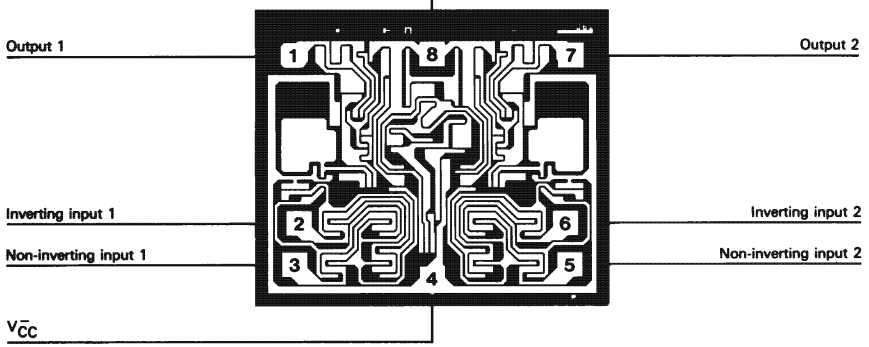
The TL062 is a low power J-FET input dual operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P791
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.61 x 1.37mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J TL062M	J TL062C	Unit
Supply voltage - (Note 1)	V_{CC}	±18	±18	V
Differential input voltage - (Note 2)	V_{ID}	±30	±30	V
Input voltage - (Note 3)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES :

1 – All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = \pm 15$ V, (Unless otherwise specified)
All characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL062M			J TL062C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S = 50\ \Omega$)	V_{IO}	–	3	6	–	3	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	nA
Input bias current*	I_{IB}	–	30	–	–	30	–	nA
Input voltage range	V_I	±11	±12	–	±10	±11	–	V
Output voltage swing ($R_L = 10$ kΩ)	V_{OPP}	20	27	–	20	27	–	V
Large signal voltage gain ($R_L \geqslant 10$ kΩ, $V_O = \pm 10$ V)	A_{VD}	4	6	–	3	6	–	V/mV
Small signal bandwidth ($R_L = 10$ kΩ)	GW_R	0.7	1	–	0.7	1	–	MHz
Common-mode rejection ratio ($R_S \leqslant 10$ kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($R_S \leqslant 10$ kΩ)	SVR	80	95	–	70	95	–	dB
Supply current (per amplifier) - (no load, no signal)	I_{CC}	–	200	250	–	200	250	μA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS.JTL062

THOMSON COMPONENTS SEMICONDUCTEURS

J TL064

LOW POWER J-FET INPUT QUAD OPERATIONAL AMPLIFIER

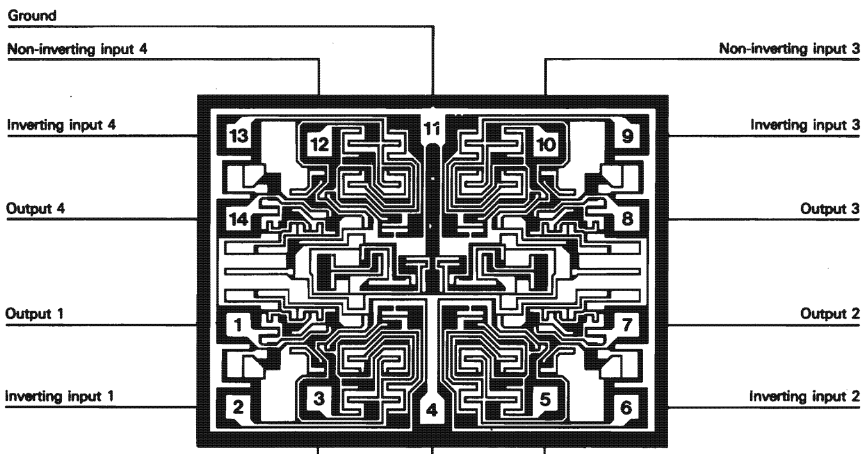
The TL064 is a low power J-FET input quad operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P737
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 2.16 x 1.64mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-2 Ceramic) TO116



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	J TL064M	J TL064C	Unit
Supply voltage - (Note 1)	V_{CC}	±18	±18	V
Differential input voltage - (Note 2)	V_{ID}	±30	±30	V
Input voltage - (Note 3)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES :

1 – All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = \pm 15$ V, (Unless otherwise specified)
All characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL064M			J TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S = 50\ \Omega$)	V_{IO}	–	3	6	–	3	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	nA
Input bias current*	I_{IB}	–	30	–	–	30	–	nA
Input common-mode voltage range	V_I	±11	±12	–	±10	±11	–	V
Output voltage swing ($R_L = 10$ kΩ)	V_{OPP}	20	27	–	20	27	–	V
Large signal voltage gain ($R_L \geqslant 10$ kΩ, $V_O = \pm 10$ V)	A_{VD}	4	6	–	3	6	–	V/mV
Small signal bandwidth ($R_L = 10$ kΩ)	GW_R	0.7	1	–	0.7	1	–	MHz
Common-mode rejection ratio ($R_S \leqslant 10$ kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$, $R_S \leqslant 10$ kΩ)	SVR	80	95	–	70	95	–	dB
Supply current (per amplifier) - (no load, no signal)	I_{CC}	–	200	250	–	200	250	μA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJTL064

THOMSON COMPONENTS SEMICONDUCTEURS

J TL071

LOW NOISE J-FET INPUT SINGLE OPERATIONAL AMPLIFIER

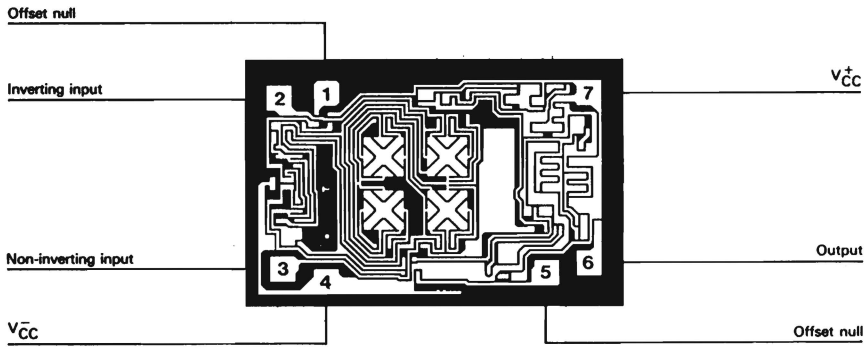
The TL071 is low power J-FET input single operational amplifier. This J-FET input operational amplifier incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P902
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.72 x 1.14mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	J TL071M	J TL071C	Unit
Supply voltage - (Note 1)	V_{CC}	± 18	± 18	V
Differential input voltage - (Note 2)	V_{ID}	± 30	± 30	V
Input voltage - (Note 3)	V_I	± 15	± 15	V
Operating free-air temperature range	T_{oper}	− 55 to + 125	0 to + 70	°C
Storage temperature range	T_{stg}	− 65 to + 150	− 65 to + 150	°C

NOTES :

1 − All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 − Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 − The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ± 15 V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL071M			J TL071C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	−	3	6	−	5	10	mV
Input offset current*	I_{IO}	−	5	−	−	5	−	pA
Input bias current*	I_{IB}	−	30	−	−	30	−	pA
Input common-mode voltage range	V_I	± 11	± 12	−	± 10	± 11	−	V
Output voltage swing ($R_L \geq$ 10 kΩ)	V_{OPP}	24	27	−	24	27	−	V
Large signal voltage gain ($R_L \geq$ 2 kΩ, V_O = ± 10 V)	A_{VD}	50	200	−	25	200	−	V/mV
Small signal bandwidth	GW_R	−	3	−	−	3	−	MHz
Common-mode rejection ratio ($R_S \geq$ 10 kΩ)	CMR	80	86	−	70	76	−	dB
Supply voltage rejection ratio ($R_S \geq$ 10 kΩ)	SVR	80	86	−	70	76	−	dB
Supply current (per amplifier)	I_{CC}	−	1.4	2.5	−	1.4	2.5	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
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Printed in France

Ref.DSJTL071

THOMSON COMPONENTS SEMICONDUCTEURS

J TL072

LOW NOISE J-FET INPUT DUAL OPERATIONAL AMPLIFIER

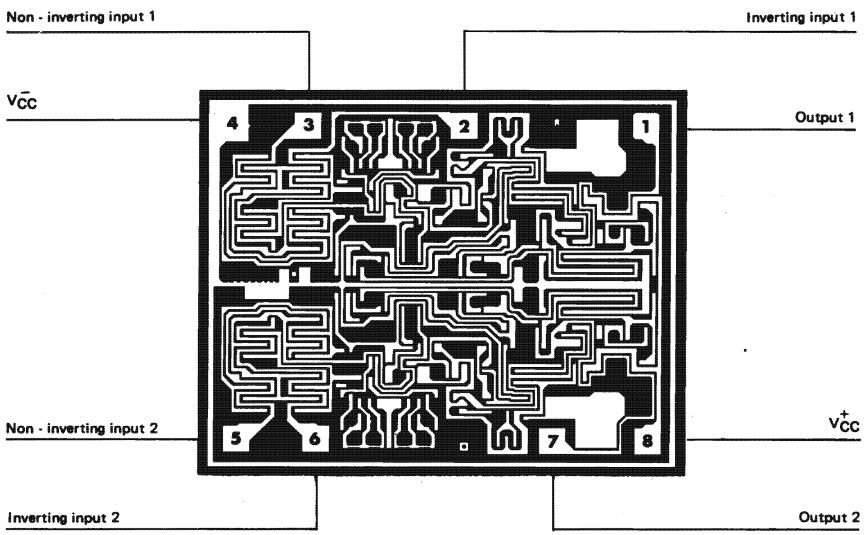
The TL072 is a low power J-FET input dual operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P856
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.70 x 2.10mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
QUALIFICATION	
LOT CASE	: (CB-11) TO99



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MAXIMUM RATINGS

Rating	Symbol	J TL072M	J TL072C	Unit
Supply voltage - (Note 1)	V_{CC}	± 18	± 18	V
Differential input voltage - (Note 2)	V_{ID}	± 30	± 30	V
Input voltage - (Note 3)	V_I	± 15	± 15	V
Operating free-air temperature range	T_{oper}	− 55 to + 125	0 to + 70	°C
Storage temperature range	T_{stg}	− 65 to + 150	− 65 to + 150	°C

NOTES :

1 – All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = ± 15 V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL072M			J TL072C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	3	6	–	5	10	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	pA
Input bias current*	I_{IB}	–	30	–	–	30	–	pA
Input common-mode voltage range	V_I	± 11	± 12	–	± 10	± 11	–	V
Output voltage swing ($R_L \geq$ 10 kΩ)	V_{OPP}	24	27	–	24	27	–	V
Large signal voltage gain ($R_L \geq$ 2 kΩ, V_O = ± 10 V)	A_{VD}	50	200	–	25	200	–	V/mV
Small signal bandwidth	GW_R	–	3	–	–	3	–	MHz
Common-mode rejection ratio ($R_S \geq$ 10 kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($R_S \geq$ 10 kΩ)	SVR	80	86	–	70	76	–	dB
Supply current (per amplifier)	I_{CC}	–	1.4	2.5	–	1.4	2.5	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref. DSJTL072

THOMSON COMPONENTS SEMICONDUCTEURS

J TL074

LOW NOISE J-FET INPUT QUAD OPERATIONAL AMPLIFIER

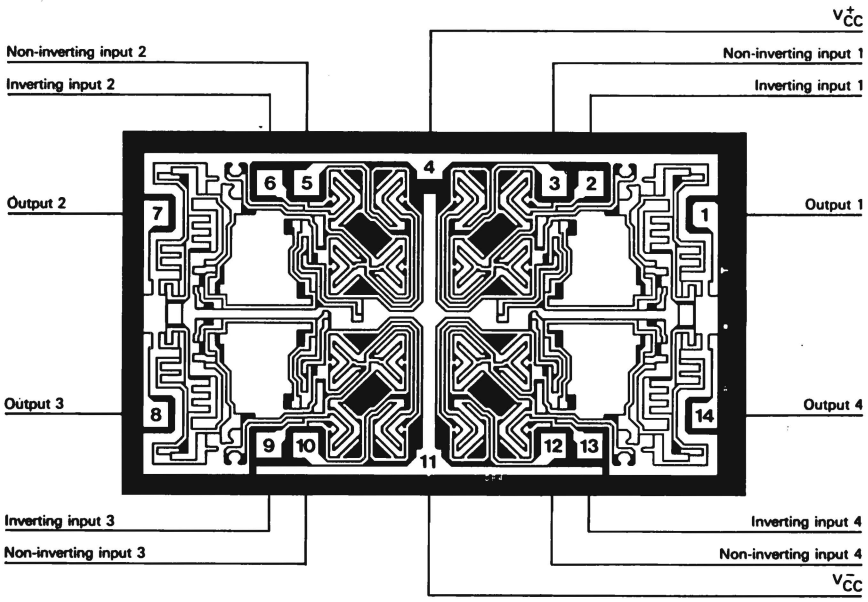
The TL074 is a low power J-FET input quad operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P878
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 2.86 x 1.69mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-2 Ceramic) TO116



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J TL074M	J TL074C	Unit
Supply voltage - (Note 1)	V_{CC}	± 18	± 18	V
Differential input voltage - (Note 2)	V_{id}	± 30	± 30	V
Input voltage - (Note 3)	V_i	± 15	± 15	V
Operating free-air temperature range	T_{oper}	− 55 to + 125	0 to + 70	°C
Storage temperature range	T_{stg}	− 65 to + 150	− 65 to + 150	°C

NOTES :

1 − All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^{+} and V_{CC}^{-}.

2 − Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 − The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ± 15 V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL074M			J TL074C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	3	6	–	5	10	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	pA
Input bias current*	I_{IB}	–	30	–	–	30	–	pA
Input common-mode voltage range	V_i	± 11	± 12	–	± 10	± 11	–	V
Output voltage swing ($R_L \geq$ 10 kΩ)	V_{OPP}	24	27	–	24	27	–	V
Large signal voltage gain ($R_L \geq$ 2 kΩ, V_O = ± 10 V)	A_{VD}	50	200	–	25	200	–	V/mV
Small signal bandwidth	GW_R	2.5	3	–	2.5	3	–	MHz
Common-mode rejection ratio ($R_S \geq$ 10 kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($R_S \geq$ 10 kΩ)	SVR	80	86	–	70	76	–	dB
Supply current (per amplifier)	I_{CC}	–	1.4	2.5	–	1.4	2.5	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/JTL074

THOMSON COMPONENTS SEMICONDUCTEURS

J TL081

J-FET INPUT SINGLE OPERATIONAL AMPLIFIER

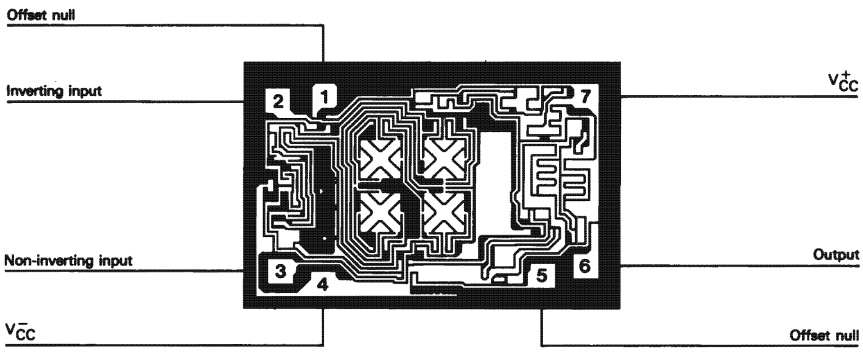
The TL081 is a high speed J-FET input single operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P902
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.72 x 1.14mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage - (Note 1)	V_{CC}	± 18	V
Differential input voltage - (Note 2)	V_{ID}	± 30	V
Input voltage - (Note 3)	V_I	± 15	V
Operating free-air temperature range J TL081C J TL081M	T_{oper}	 0 to + 70 − 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

NOTES :

1 – All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 – Differential voltage are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = ± 15 V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL081M			J TL081C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (R_S = 50 Ω)	V_{IO}	–	3	6	–	5	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	pA
Input bias current*	I_{IB}	–	30	–	–	30	–	pA
Input common-mode voltage range	V_I	± 11	± 12	–	± 10	± 11	–	V
Output voltage swing (R_L ⩾ 10 kΩ)	V_{OPP}	24	27	–	24	27	–	V
Large signal voltage gain (R_L ⩾ 2 kΩ, V_O = ± 10 V)	A_{VD}	50	200	–	25	200	–	V/mV
Small signal bandwidth	GW_R	–	3	–	–	3	–	MHz
Common-mode rejection ratio (R_S ⩾ 10 kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio (R_S ⩾ 10 kΩ)	SVR	80	86	–	70	76	–	dB
Supply current (per amplifier)	I_{CC}	–	1.4	2.8	–	1.4	2.8	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/TL081

THOMSON COMPONENTS SEMICONDUCTEURS

J TL082

J-FET INPUT DUAL OPERATIONAL AMPLIFIER

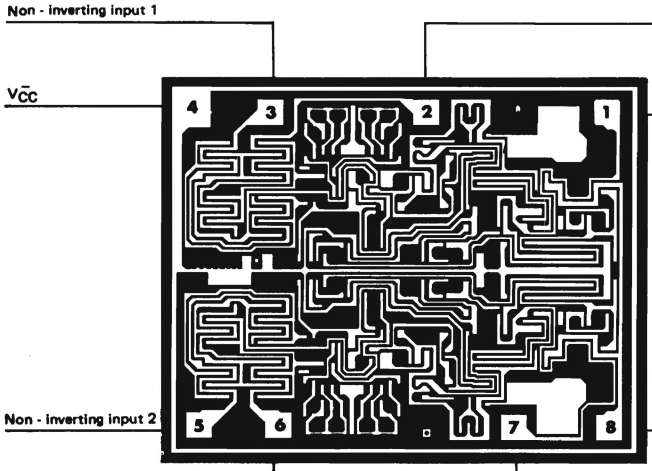
The TL082 is a high speed J-FET input dual operational amplifier incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P856
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.70 x 2.10mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage - (Note 1)	V_{CC}	±18	V
Differential input voltage - (Note 2)	V_{ID}	±30	V
Input voltage - (Note 3)	V_I	±15	V
Operating free-air temperature range J TL082C J TL082M	T_{oper}	 0 to + 70 −55 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

NOTES :

1 – All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = \pm 15$ V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL082M			J TL082C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S = 50\ \Omega$)	V_{IO}	–	3	6	–	5	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	pA
Input bias current*	I_{IB}	–	30	–	–	30	–	pA
Input voltage range	V_I	±11	±12	–	±10	±11	–	V
Output voltage swing ($R_L \geq 10$ kΩ)	V_{OPP}	24	27	–	24	27	–	V
Large signal voltage gain ($R_L \geq 2$ kΩ, $V_O = \pm 10$ V)	A_{VD}	50	200	–	25	200	–	V/mV
Small signal bandwidth	GW_R	–	3	–	–	3	–	MHz
Common-mode rejection ratio ($R_S \geq 10$ kΩ)	CMR	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($R_S \geq 10$ kΩ)	SVR	80	86	–	70	76	–	dB
Supply current (per amplifier)	I_{CC}	–	1.4	2.8	–	1.4	2.8	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.:DSJTL082

THOMSON COMPONENTS SEMICONDUCTEURS

J TL084

J-FET INPUT QUAD OPERATIONAL AMPLIFIER

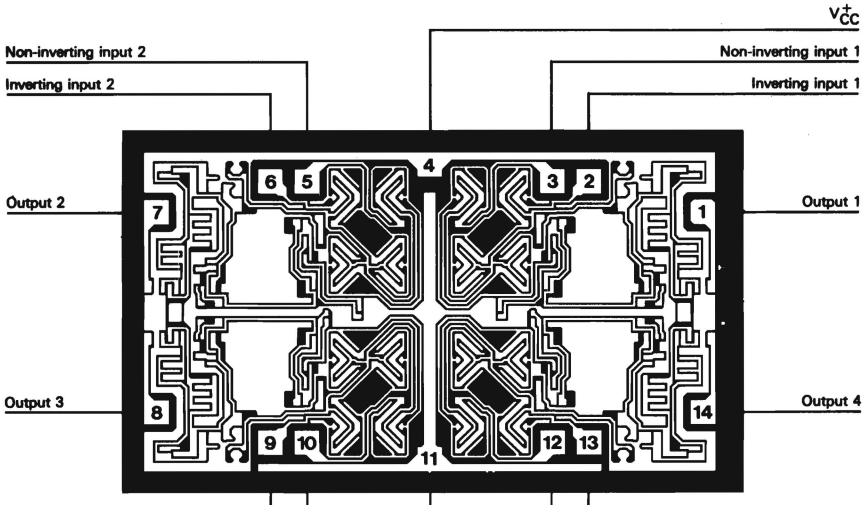
The TL084 is a high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

J-FET

SPECIFICATIONS

PAD LAYOUT	: P878
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 2.86 x 1.69mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al - Cu (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-2 Ceramic) TO116



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage - (Note 1)	V_{CC}	±18	V
Differential input voltage - (Note 2)	V_{ID}	±30	V
Input voltage - (Note 3)	V_I	±15	V
Operating free-air temperature range J TL084C J TL084M	T_{oper}	 0 to + 70 −55 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

NOTES :

1 – All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^{+} and V_{CC}^{-}.

2 – Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.

3 – The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = \pm 15$ V, (Unless otherwise specified)
Test conditions : all characteristics are specified under open-loop conditions unless otherwise specified.

Characteristic	Symbol	J TL084M			J TL084C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S = 50\ \Omega$)	V_{IO}	–	3	6	–	5	15	mV
Input offset current*	I_{IO}	–	5	–	–	5	–	pA
Input bias current*	I_{IB}	–	30	–	–	30	–	pA
Input voltage range	V_I	±11	±12	–	±10	±11	–	V
Output voltage swing ($R_L \geq 10$ kΩ)	V_{OPP}	24	27	–	24	27	–	V
Large signal voltage gain ($R_L \geq 2$ kΩ, $V_O = \pm 10$ V)	A_{VD}	50	200	–	25	200	–	V/mV
Small signal bandwidth	GW_R	2.5	3	–	2.5	3	–	MHz
Common-mode rejection ratio ($R_S \geq 10$ kΩ)	CM_R	80	86	–	70	76	–	dB
Supply voltage rejection ratio ($R_S \geq 10$ kΩ)	SVR	80	86	–	70	76	–	dB
Supply current (per amplifier)	I_{CC}	–	1.4	2.8	–	1.4	2.8	mA

* Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

Ref.DS.JTL084

THOMSON COMPONENTS SEMICONDUCTEURS

J UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

The UA741 is a high performance monolithic operational amplifier. It is intended for a wide range of analog applications.

- Summing amplifier.
- Voltage follower.
- Integrator.
- Active filter.
- Function generator.

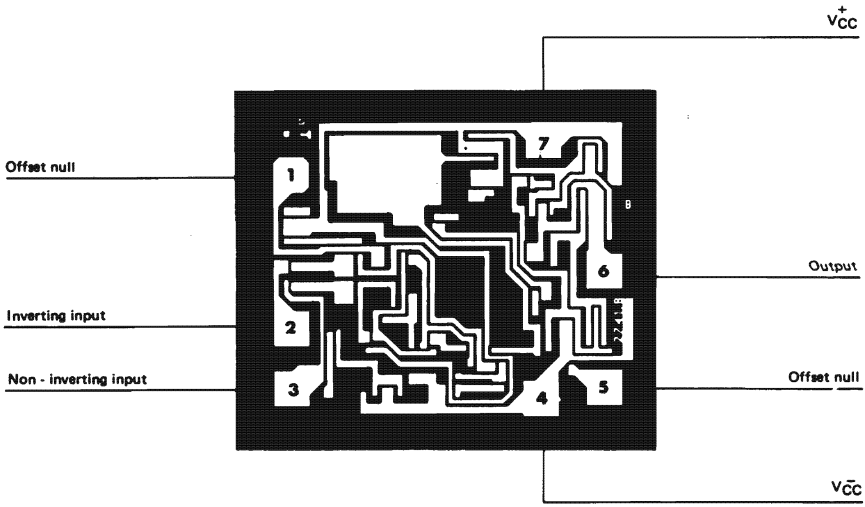
The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The internal compensation network (6 dB/octave) insures stability in closed loop applications.

- Large input voltage range.
- No latch-up.
- High gain.
- Short-circuit protection.
- No frequency compensation required.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P728
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.32 x 1.12mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: TO99



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	J UA741M	J UA741C	Unit
Supply voltage	V_{CC}	±22	±18	V
Differential input voltage	V_{ID}	±30	±30	V
Input voltage	V_I	±18	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ±15 V, (Unless otherwise specified)

Characteristic	Symbol	J UA741M			J UA741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1	5	–	2	6	mV
Input offset current	I_{IO}	–	20	200	–	20	200	nA
Input bias current	I_{IB}	–	80	500	–	80	500	nA
Large signal voltage gain (V_O = ±10 V, $R_L \geq 2$ kΩ)	A_{VD}	50	200	–	20	200	–	V/mV
Supply voltage rejection ratio ($R_S \leq 10$ kΩ)	SVR	–	30	150	–	30	150	μV/V
Supply current	I_{CC}^+, I_{CC}^-	–	1.7	2.8	–	1.7	2.8	mA
Input voltage range	V_I	±12	±13	–	±12	±13	–	V
Common-mode rejection ratio ($R_S \leq 10$ kΩ)	CMR	70	90	–	70	90	–	dB
Output voltage swing $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	V_{OPP}	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJUA741

THOMSON COMPONENTS SEMICONDUCTEURS

J UA776

PROGRAMMABLE SINGLE OPERATIONAL AMPLIFIER

The UA776 programmable operational amplifier is characterized by high input impedance, low supply currents and low input noise over a wide range of operating supply voltages.

Coupled with programmable electrical characteristics it is an extremely versatile amplifier for use in high accuracy, low power consumption analog applications.

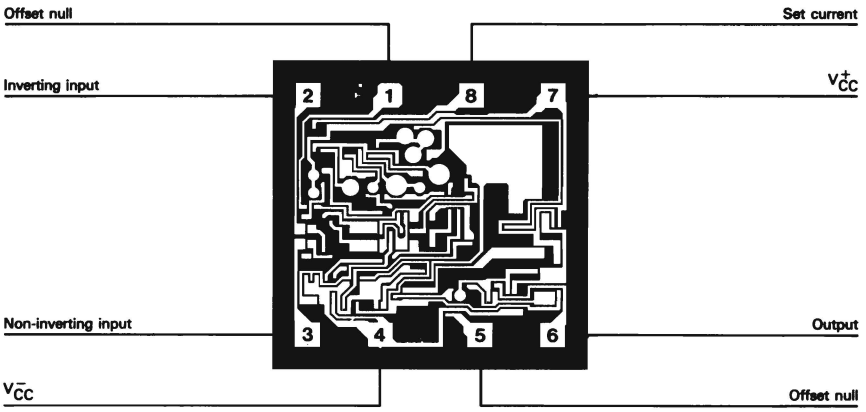
Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the UA741.

Internal frequency compensation, absence of latch up, high slew rate and short-circuit protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	XO21
PAD SIZE	:	0.12 x 0.12mm
DIE SIZE	:	1.43 x 1.43mm
DIE THICKNESS	:	0.375mm ± 0.025
METALLIZATION	:	Al (front side)
PASSIVATION	:	Nitride
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		J UA776M	J UA776C	
Supply voltage	V_{CC}	±18	±18	V
Differential input voltage	V_{ID}	±30	±30	V
Input voltage - (Note 1)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

Note 1 : For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ± 15 V, I_{set} = 15 μA, (Unless otherwise specified)

Characteristic	Symbol	J UA776M			J UA776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	V_{IO}	—	2	5	—	2	6	mV
Input offset current	I_{IO}	—	2	15	—	2	25	nA
Input bias current	I_{IB}	—	15	50	—	15	50	nA
Large signal voltage gain (V_O = ± 10 V, $R_L \geq 5$ kΩ)	A_{VD}	10^5	4.10^5	—	5.10^4	4.10^5	—	V/V
Supply voltage rejection ratio ($R_S \leq 10$ kΩ)	SVR	—	25	150	—	25	200	μV/V
Supply current	I_{CC}	—	160	180	—	160	190	μA
Input voltage range	V_I	± 10	—	—	± 10	—	—	V
Common-mode rejection ratio ($R_S \leq 10$ kΩ)	CMR	70	90	—	70	90	—	dB
Output voltage swing ($R_L \geq 5$ kΩ)	V_{OPP}	± 10	± 13	—	± 10	± 13	—	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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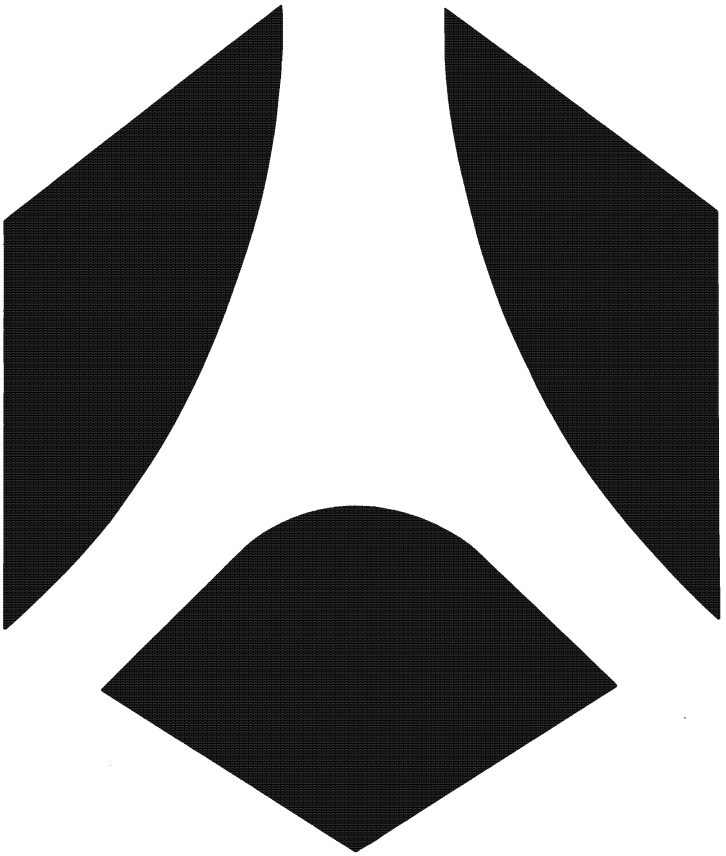
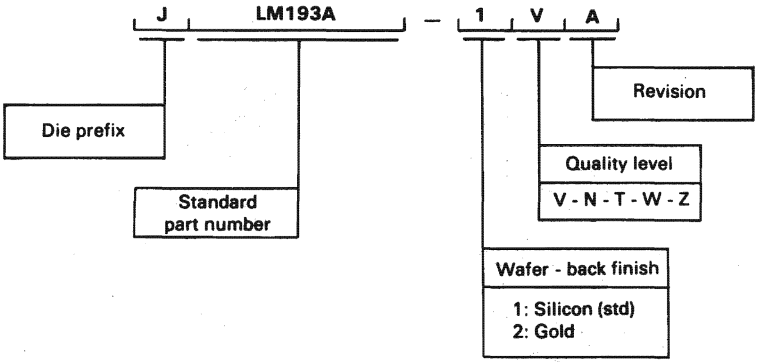
Ref.DSJUA776



Voltage comparators

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J LM111		X	X	X	X	X	X	X	A
J LM311		X	X	X			X	X	A
J LM119		X	X	X	X	X	X	X	A
J LM319		X	X	X			X	X	A
J LM139		X	X	X	X	X		X	A
J LM339		X	X	X				X	A
J LM139A		X	X	X	X	X		X	A
J LM339A		X	X	X				X	A
J LM193		X	X	X	X	X	X	X	A
J LM393		X	X	X			X	X	A
J LM193A		X	X	X	X	X	X	X	A
J LM393A		X	X	X			X	X	A

THOMSON COMPONENTS SEMICONDUCTEURS

J LM111 • J LM311

SINGLE VOLTAGE COMPARATOR

The LM111, and LM311 are voltage comparators that have extremely low input currents.

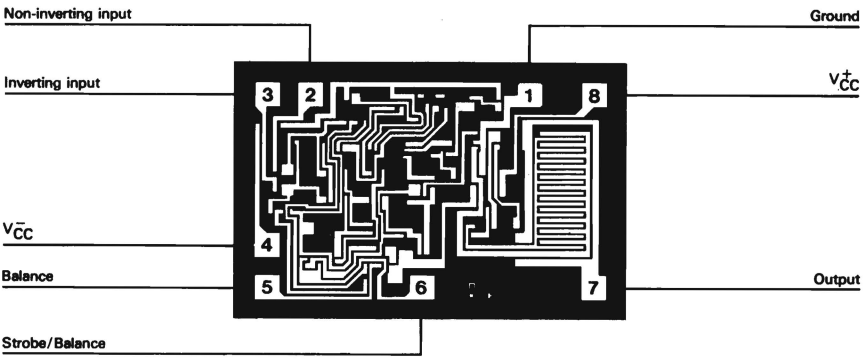
They are also designed to operate over a wide range of supply voltages : from standard ±15 V operational amplifier supplies down to the single +5 V supply used for IC logic.

Their output is compatible with RTL-DTL and TTL as well as MOS circuits and can switch voltages up to +50 V at output currents as high as 50mA.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P854
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 1.18 x 1.78mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-11) TO99



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	J LM111	J LM311	Unit
Supply voltage	V_{CC}	36	36	V
Differential input voltage	V_{ID}	±30	±30	V
Input voltage - (Note 1)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C
Ground to negative supply voltage	$V_{(1-4)}$	30	30	V
Output to negative supply voltage	$V_{(7-4)}$	50	40	V

Voltage at strobe pin : V_{CC}^{+} − 5 V

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = ±15 V, (Unless otherwise specified) (Note 2)

Characteristic	Symbol	J LM111			J LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 50$ kΩ) - (Note 3)	V_{IO}	—	0.7	3	—	2	7.5	mV
Input offset current - (Note 3)	I_{IO}	—	4	10	—	6	50	nA
Input bias current	I_{IB}	—	60	100	—	100	250	nA
Large signal voltage gain	A_{VD}	40	200	—	40	200	—	V/mV
Supply currents Positive Negative	 I_{CC}^{+} I_{CC}^{-}	 — —	 5.1 4.1	 6 5	 — —	 5.1 4.1	 7.5 5	mA
Input voltage range	V_I	—	±14	—	—	±14	—	V
Low level output voltage I_O = 50 mA, $V_I \leq -5$ mV $V_I \leq -10$ mV	V_{OL}	 — —	 0.75 —	 1.5 —	 — —	 — 0.75	 — 1.5	V
High level output current $V_I \geq +5$ mV, V_O = +35 V $V_I \geq +10$ mV, V_O = +25 V	I_{OH}	 — —	 0.2 —	 10 —	 — —	 — 0.2	 — 50	nA

NOTES :

1 – This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

2 – The offset voltage, offset current and bias current specifications apply for any supply voltage from a single +5 V supply up to ±15 V supplies.

3 – The offset voltage and offset currents given are the maximum values required to drive the output down to +1 V or up to +14 V with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case of voltage gain and input impedance.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJLM111JLM311

THOMSON COMPONENTS SEMICONDUCTEURS

J LM119 • J LM319

HIGH SPEED DUAL COMPARATOR

The LM119, LM319 are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5 V logic supply and ground and have extremely low input currents and high gains.

The open collector of the output stage makes the LM119, LM319 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

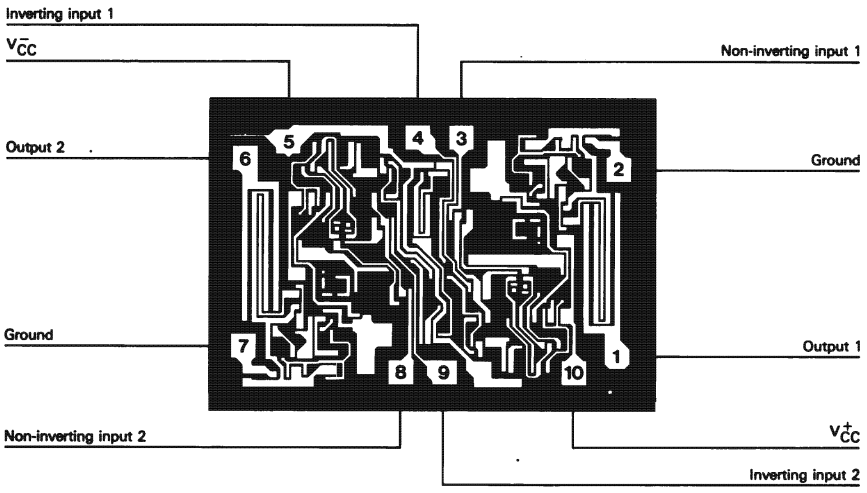
Although designed primarily for applications requiring operation from digital logic supplies, the LM119, LM319 are fully specified for power supplies up to ±15 V.

They feature faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range make the LM119, LM319 much more versatile.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P886
PAD SIZE	: 0.12 x 0.12mm
DIE SIZE	: 2.03 x 1.43mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Nitride
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-3) TO100



Back side bias : V_{CC}^-

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MAXIMUM RATINGS

Rating	Symbol	J LM119	J LM319	Unit
Negative supply voltage	V_{CC}^-	25	25	V
Positive supply voltage	V_{CC}^+	18	18	V
Differential input voltage	V_{ID}	±5	±5	V
Input voltage - (Note 1)	V_I	±15	±15	V
Operating free-air temperature range	T_{oper}	−55 to +125	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (Note 2)

T_{amb} = +25°C, V_{CC} = ±15 V, (Unless otherwise specified)

Characteristic	Symbol	J LM119			J LM319			Unit
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ($R_S \leq 5$ kΩ) - (Note 3)	V_{IO}	–	0.7	4	–	2	8	mV
Input offset current - (Note 3)	I_{IO}	–	30	75	–	80	200	nA
Input bias current	I_{IB}	–	150	500	–	250	1000	nA
Large signal voltage gain	A_{VD}	10	40	–	8	40	–	V/mV
Positive supply current V_{CC}^+ = +5 V, V_{CC}^- = 0 V	I_{CC}^+	– –	8 4.3	11.5 –	– –	8 4.3	12.5 –	mA
Negative supply current	I_{CC}^-	–	3	4.5	–	3	5	mA
Input voltage range (V_{CC}^+ = +5 V, V_{CC}^- = 0 V)	V_I	– 1	±13 –	– 3	– 1	±13 –	– 3	V
Low level output voltage, (I_O = 25 mA) V_I < − 5 mV V_I < −10 mV V_{CC}^+ > +4.5 V, V_{CC}^- = 0 V, V_I < − 6 mV, $I_{O(sink)}$ < 3.2 mA V_{CC}^+ > +4.5 V, V_{CC}^- = 0 V, V_I < −10 mV, $I_{O(sink)}$ < 3.2 mA	V_{OL}	– – – –	0.75 – 0.23 –	1.5 – 0.4 –	– – – –	– 0.75 – 0.3	– 1.5 – 0.4	V
High level output current (V_O = +35 V) V_I > + 5 mV V_I > +10 mV	I_{OH}	– –	0.2 –	2 –	– –	– 0.2	– 10	μA

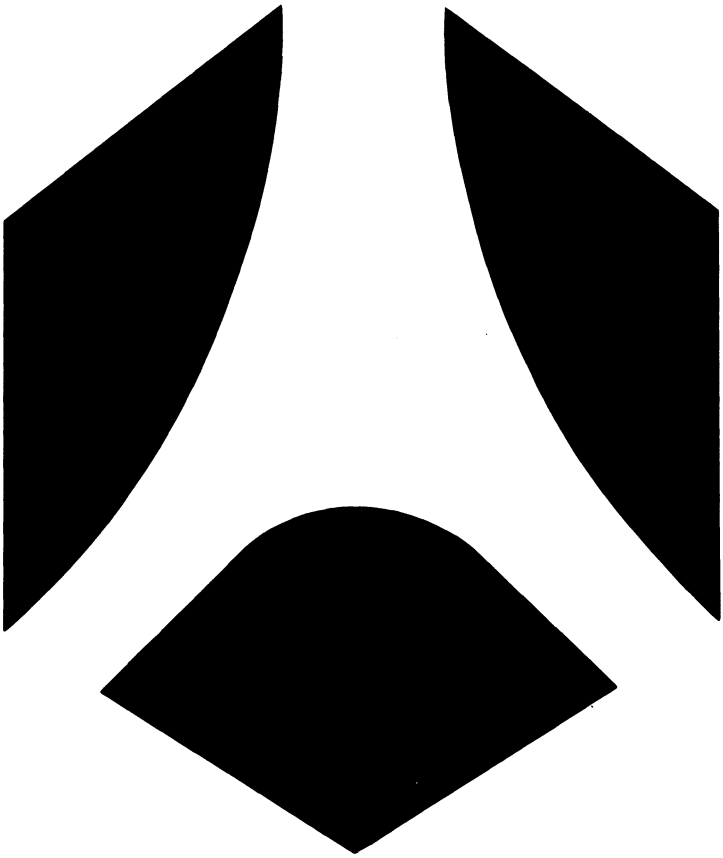
NOTES :

1 – For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

2 – These specifications apply for V_{CC} = ±15 V, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single +5 V supply up to ±15 V supplies.

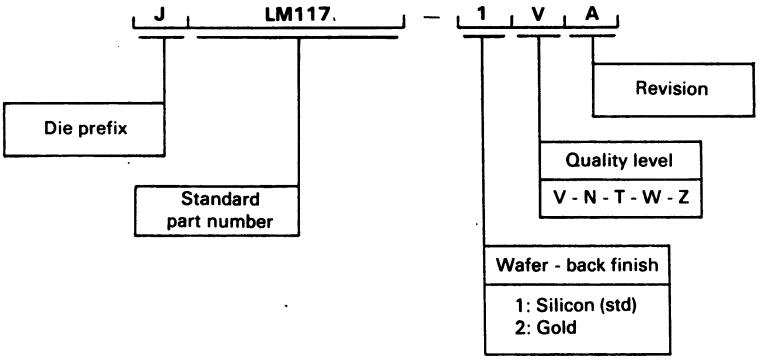
3 – The offset voltages and offset current given are the maximum values required to drive the output down to 1 V or up 14 V with a 1 mA load current.
Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Ref.DS/LM119/LM319



Voltage regulators

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J LM117		X	X	X	X	X	X	X	A
J LM317		X	X	X			X	X	A
J LM137		X	X	X	X	X	X	X	A
J LM337		X	X	X			X	X	A
J LM138		X						X	A
J LM338		X						X	A
J UA723		X	X	X	X	X	X	X	A
J UA7805		X	X	X	X	X	X	X	A
J UA7812		X	X	X	X	X	X	X	A
J UA7815		X	X	X	X	X	X	X	A
J UA7905		X	X	X	X	X	X	X	A
J UA7912		X	X	X	X	X	X	X	A
J UA7915		X	X	X	X	X	X	X	A

THOMSON COMPONENTS SEMICONDUCTEURS

J LM117 • J LM317

THREE TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

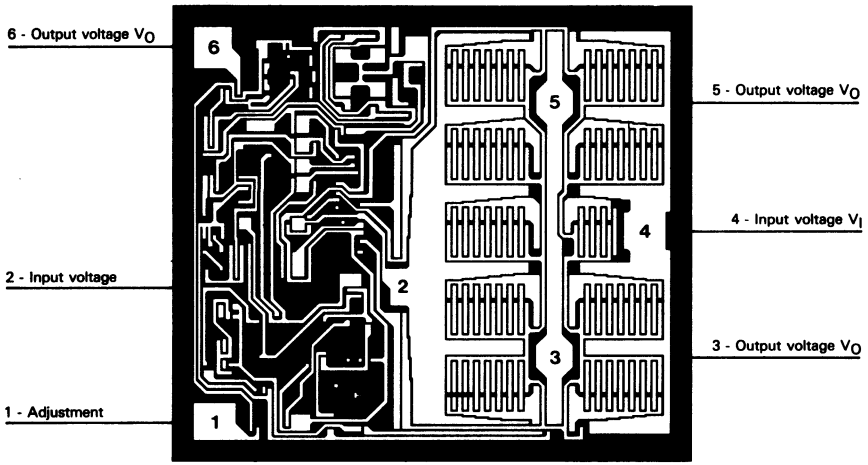
The LM117 series are adjustable positive voltage regulators capable of supplying in excess of 1.5 A over a 1.2 to 37 V output voltage range. They are exceptionnally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators.

In addition to higher performance than fixed regulators, the LM117 series offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P378
PAD SIZE	: 0.18 x 0.20mm
DIE SIZE	: 2.40 x 2.15mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-7) TO39



Back side bias : $V_{\overline{CC}}$

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input - Output voltage differential	$V_I - V_O$	40	V
Output current	I_O	1.5	A
Operating junction temperature range J LM117 J LM317	T_j	 −55 to +150 0 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_j = +25°C$, $V_I - V_O = 5$ V, $I_O = 0.5$ A
(Unless otherwise specified)

Characteristic	Symbol	J LM117			J LM317			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference voltage (10 mA ≤ I_O ≤ 0.5 A, 3 V ≤ $V_I - V_O$ ≤ 40 V) -(Note 1)	$V_{(ref)}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line regulation (I_O = 0.1 A, 3 V ≤ $V_I - V_O$ ≤ 40 V) -(Note 1)	K_{VI}	—	0.01	0.02	—	0.01	0.04	%/V
Load regulation, (10 mA ≤ I_O ≤ 0.5 A) -(Note 1) V_O ≤ +5 V V_O ≥ +5 V	K_{VO}	 — —	 5 0.1	 15 0.3	 — —	 5 0.1	 25 0.5	 mV %
Adjustment pin current	I_{adj}	—	50	100	—	50	100	µA
Adjustment pin current change (10 mA ≤ I_O ≤ 0.5 A, 3 V ≤ $V_I - V_O$ ≤ 40 V)	ΔI_{adj}	—	0.2	5	—	0.2	5	µA
Minimum load current ($V_I - V_O$ = 40 V)	$I_{O(min)}$	—	3.5	5	—	3.5	10	mA

NOTE :

1 – Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJLM117/LM317

THOMSON COMPONENTS SEMICONDUCTEURS

J LM137 • J LM337

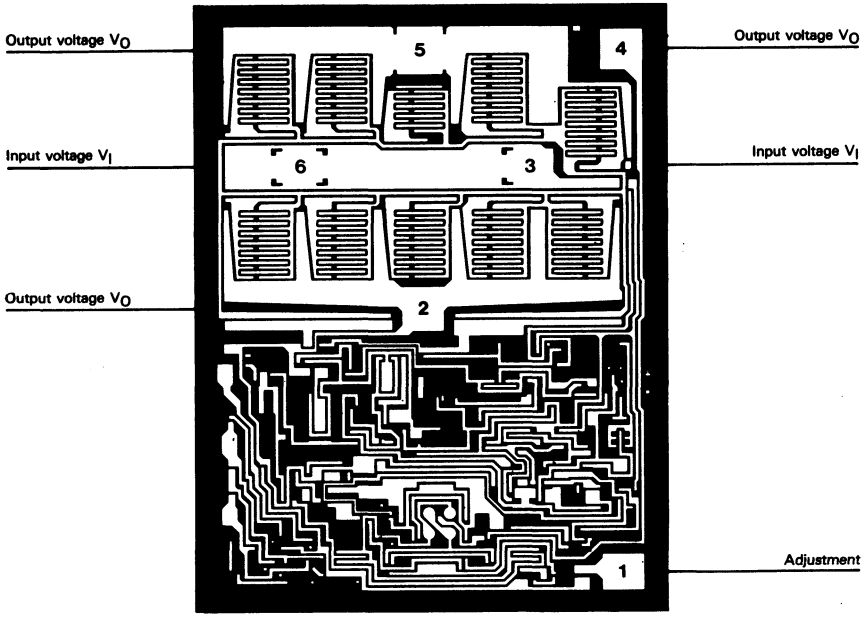
THREE TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

The LM137 series are adjustable negative voltage regulators capable of supplying in excess of −1.5 A over a −1.2 to −37 V output voltage range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. In addition to higher performance than fixed regulators, the LM137 series offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P462
PAD SIZE	: 0.2 x 0.2mm
DIE SIZE	: 2.18 x 2.87mm
DIE THICKNESS	: 0.375mm ± 0 025
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-7) TO39



Back side bias : V_{CC}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input - Output voltage differential	$V_I - V_O$	40	V
Output current	I_O	1.5	A
Operating junction temperature range J LM137 J LM337	T_j	 −55 to +150 0 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_j = +25°C$, $|V_I - V_O| = 5$ V, $I_O = 0.5$ A
(Unless otherwise specified)

Characteristic	Symbol	J LM137			J LM337			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference voltage (3 V ≤ $\|V_I - V_O\|$ ≤ 40 V, 10 mA < $\|I_O\|$ < 0.5 A)	V_{ref}	−1.20	−1.25	−1.30	−1.20	−1.25	−1.30	V
Line regulation (3 V ≤ $\|V_I - V_O\|$ ≤ 40 V) -(Note 1)	K_{VI}	—	0.01	0.02	—	0.01	0.04	%/V
Load regulation (10 mA ≤ $\|I_O\|$ ≤ 0.5 A) -(Note 1) $\|V_O\|$ ≤ 5 V $\|V_O\|$ ≥ 5 V	K_{VO}	 — —	 15 0.3	 25 0.5	 — —	 15 0.3	 50 1	 mV %
Adjustment pin current	I_{adj}	—	65	100	—	65	100	μA
Adjustment pin current change (10 mA ≤ $\|I_O\|$ ≤ 0.5 A, 3 V ≤ $\|V_I - V_O\|$ ≤ 40 V)	ΔI_{adj}	—	2	5	—	2	5	μA
Minimum load current ($\|V_I - V_O\|$ ≤ 40 V)	$\|I_{O(min)}\|$	—	2.5	5	—	2.5	10	mA

NOTE :

1 – Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Printed in France

Ref.DSJLM137JLM337

THOMSON COMPONENTS SEMICONDUCTEURS

J LM138 • J LM338

THREE TERMINAL 5A ADJUSTABLE VOLTAGE REGULATOR

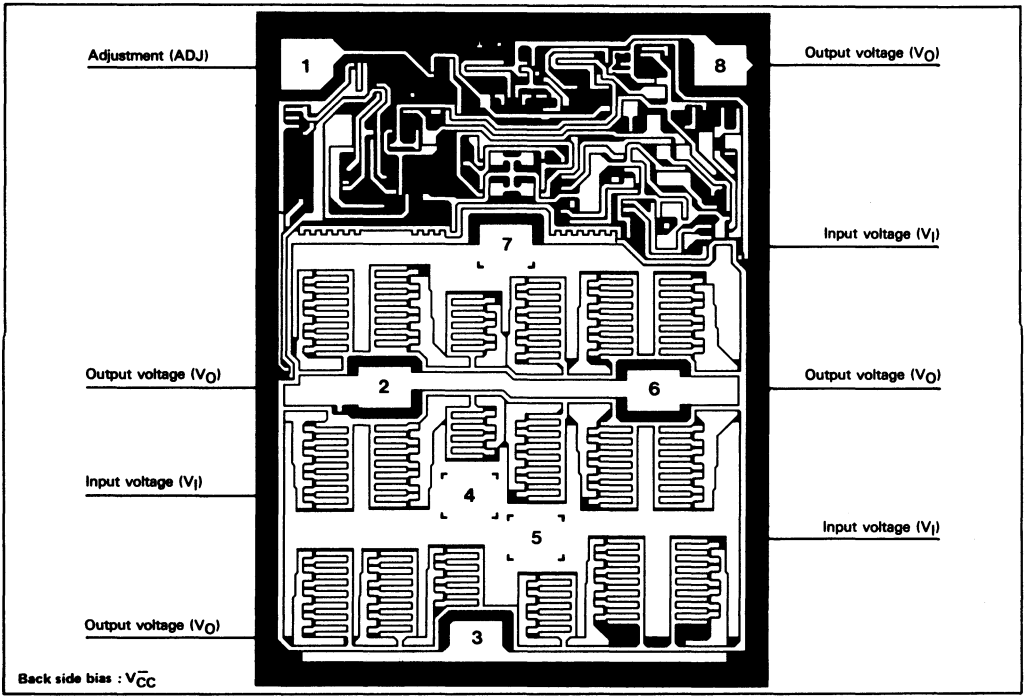
The LM138/LM338 are adjustable positive voltage regulators capable of supplying in excess of 5 A over a 1.2 V to 32 V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage.

Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment terminal is accidentally disconnected.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	XO45
PAD SIZE	:	0.20 x 0.25mm
DIE SIZE	:	2.36 x 3.18mm
DIE THICKNESS	:	0.375mm ± 0 025
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-19) TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Output voltage range	V_O	1.2 to 32	V
Input/Output voltage differential	$V_I - V_O$	35	V
Operating junction temperature range J LM138 J LM338	T_j	 −55 to +150 0 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_j = +25°C$, (Unless otherwise specified)

Characteristic	Symbol	J LM138			J LM338			Unit
		Min	Typ	Max	Min	Typ	Max	
Line regulation ($+3\ V \leq (V_I - V_O) \leq +35\ V$) -(Note 1)	K_{VI}	—	0.005	0.01	—	0.005	0.03	%/V
Load regulation ($10\ mA \leq I_O \leq 3\ A$) -(Note 1) $V_O \leq +5\ V$ $V_O \geq +5\ V$	K_{VO}	 — —	 5 0.1	 15 0.3	 — —	 5 0.1	 25 0.5	 mV %
Adjustment pin current	I_{adj}	—	45	100	—	45	100	μA
Adjustment pin current change $10\ mA \leq I_L \leq 3\ A$; $+3\ V \leq (V_I - V_O) \leq +35\ V$	ΔI_{adj}	—	0.2	5	—	0.2	5	μA
Reference voltage ($+3\ V \leq (V_I - V_O) \leq +35\ V$, $10\ mA \leq I_O \leq 3\ A$)	$V_{(ref)}$	1.19	1.24	1.29	1.19	1.24	1.29	V
Minimum load current ($V_I - V_O = +35\ V$)	$I_{O(min)}$	—	3.5	5	—	3.5	10	mA

NOTE :

1 – Regulation is measured at constant junction temperature. Change in output voltage due to heating effects are taken into account separately by thermal regulation.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.:DS/LM138/LM338

THOMSON COMPONENTS SEMICONDUCTEURS

J UA723

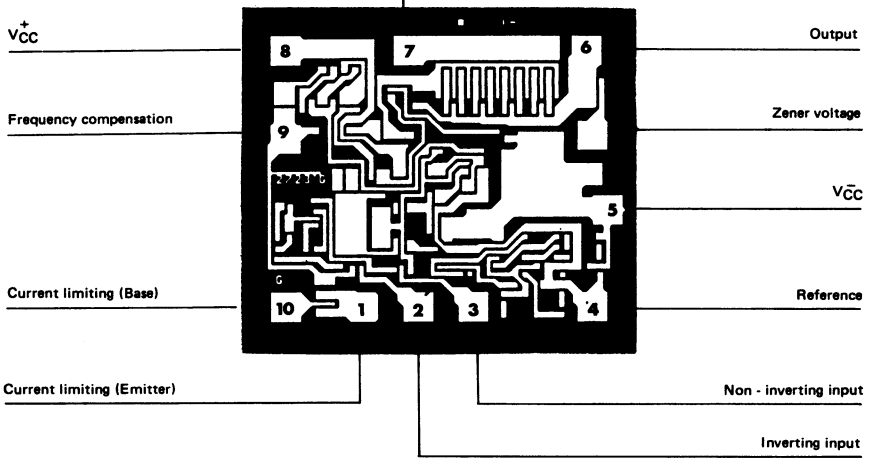
PRECISION ADJUSTABLE VOLTAGE REGULATOR

The UA723 is a monolithic voltage regulator constructed on single silicon chip. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shut down. In addition to the above the device features low standby current drain, low temperature drift and high ripple rejection. Applications include laboratory power supplies, airborne systems and other power supplies for digital and linear circuits.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	P904
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	1.28 x 1.13mm
DIE THICKNESS	:	0.375mm ± 0.025
METALLIZATION	:	Al (front side)
PASSIVATION	:	Nitride
REVISION	:	A
QUALIFICATION		
LOT CASE	:	TO100



Back side bias : $V_{\overline{CC}}$

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage (Both inputs)	V_I	40	V
Pulse voltage from V_{CC}^+ to V_{CC}^- (50 ms)	$V_{I(pulse)}$	50	V
Input-output voltage differential	$V_I - V_O$	38	V
Output current	I_O	150	mA
Operating junction temperature range J UA723C J UA723M	T_j	 0 to + 70 −55 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, $T_j = +25°C$, $V_I = V_{CC}^+ = V_C = +12$ V, $V_{CC}^- = 0$, $V_O = +5$ V, $I_C = 1$ mA, $R_{SC} = 0$, C_1 (compensation) = 100 pF and divider impedance as seen by error amplifier ⩽ 10 kΩ.

Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Characteristic	Symbol	J UA723M			J UA723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input voltage range	V_I	9.5	—	40	9.5	—	40	V
Output voltage range	V_O	2	—	37	2	—	37	V
Input-output voltage differential	$V_I - V_O$	3	—	38	3	—	38	V
Line regulation +12 V ⩽ V_I ⩽ +15 V +12 V ⩽ V_I ⩽ +40 V	K_{VI}	 — —	 0.01 0.02	 0.1 0.2	 — —	 0.01 0.1	 0.1 0.5	%/V_O
Load regulation (1 mA ⩽ I_O ⩽ 50 mA)	K_{VO}	—	0.03	0.15	—	0.03	0.2	%/V_O
Standby current drain ($I_O = 0$, $V_I = +30$ V)	I_{IB}	—	2.3	3.5	—	2.3	4	mA
Reference voltage	$V_{(ref)}$	6.95	7.15	7.35	6.8	7.15	7.5	V
Short-circuit current ($R_{SC} = 10\ \Omega$, $V_O = 0$)	I_{SC}	—	65	—	—	65	—	mA

Ref.DSJUA723

THOMSON COMPONENTS SEMICONDUCTEURS

J UA7805 • J UA7812 • JUA7815

FIXED POSITIVE VOLTAGE REGULATORS

This series of regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

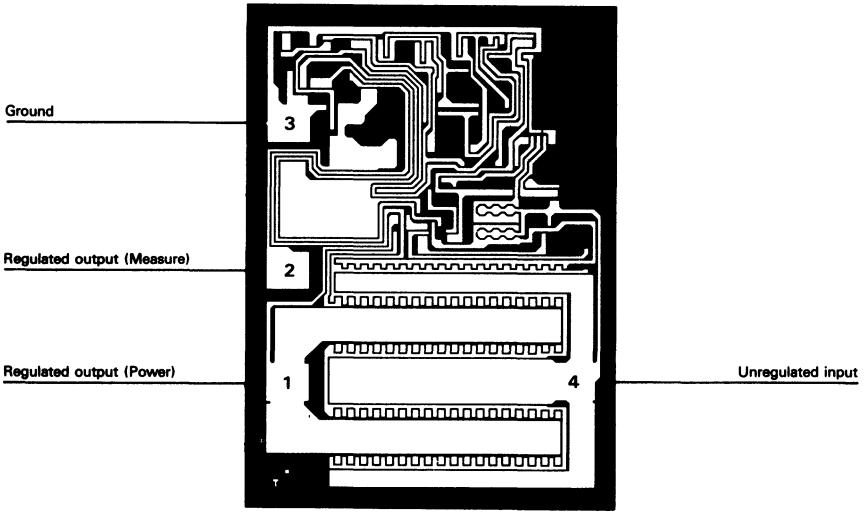
Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If power dissipation becomes too high, the thermal shutdown circuit takes over preventing the chip form over-heating.

Considerable effort was expended to make this series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P414
PAD SIZE	: 0.20 x 0.18mm
DIE SIZE	: 1.71 x 2.38mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-7) TO39



Back side bias : V_{CC}^{-}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage	V_I	35	V
Output current	I_O	Internally limited	A
Junction temperature	T_j	+150	°C
Operating temperature range J UA7805/12/15C J UA7805/12/15M	T_{oper}	 0 to +150 −55 to +150	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_j = +25°C, V_I = +10 V, I_O = 0.5 A, (Unless otherwise specified)

Characteristic	Symbol	J UA7805C			J UA7805M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range (5 mA≤I_O≤0.5 A)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	V
Line regulation -(Note 1) +8 V≤V_I≤ +12 V +7 V≤V_I≤ +25 V	K_{VI}	 – –	 – –	 50 100	 – –	 – –	 25 50	mV
Load regulation (5 mA≤I_O≤0.5 A) -(Note 1)	K_{VO}	–	–	100	–	–	50	mV
Quiescent current	I_{IB}	–	6	10	–	5.5	8	mA
Quiescent current change +8 V≤V_I≤ +25 V +7 V≤V_I≤ +25 V 5 mA≤I_O≤0.5 A	ΔI_{IB}	 – – –	 – – –	 – 1.3 0.5	 – – –	 – – –	 0.8 – 0.5	mA

NOTE :

1 – Load and line regulation are specified at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

ELECTRICAL OPERATING CHARACTERISTICS

T_j = +25°C, V_I = +19 V, I_O = 0.5 A, (Unless otherwise specified)

Characteristic	Symbol	J UA7812C			J UA7812M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range (5 mA ≤ I_O ≤ 0.5 A)	V_O	11.5	12	12.5	11.5	12	12.5	V
Line regulation - Note 2	K_{VI}							mV
+16 V ≤ V_I ≤ +22 V		–	–	120	–	–	60	
+14.5 V ≤ V_I ≤ +30 V		–	–	240	–	–	120	
Load regulation (5 mA ≤ I_O ≤ 0.5 A) -(Note 2)	K_{VO}	–	–	240	–	–	120	mV
Quiescent current	I_{IB}	–	6	10	–	5.5	8	mA
Quiescent current change	ΔI_{IB}							mA
+15 V ≤ V_I ≤ +30 V, I_O = 0.5 A		–	–	–	–	–	0.8	
+14.5 V ≤ V_I ≤ +30 V, I_O = 0.5 A		–	–	1.3	–	–	–	
5 mA ≤ I_O ≤ 0.5 A		–	–	0.5	–	–	0.5	

ELECTRICAL OPERATING CHARACTERISTICS

T_j = +25°C, V_I = +23 V, I_O = 0.5 A, (Unless otherwise specified)

Characteristic	Symbol	J UA7815C			J UA7815M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range (5 mA ≤ I_O ≤ 0.5 A)	V_O	14.4	15	15.6	14.4	15	15.6	V
Line regulation - Note 2	K_{VI}							mV
+20 V ≤ V_I ≤ +26 V		–	–	150	–	–	75	
+17.5 V ≤ V_I ≤ +30 V		–	–	300	–	–	150	
Load regulation (5 mA ≤ I_O ≤ 0.5 A) -(Note 2)	K_{VO}	–	–	300	–	–	150	mV
Quiescent current	I_{IB}	–	6	10	–	5.5	8	mA
Quiescent current change	ΔI_{IB}							mA
+18.5 V ≤ V_I ≤ +30 V		–	–	–	–	–	0.8	
+17.5 V ≤ V_I ≤ +30 V		–	–	1	–	–	–	
5 mA ≤ I_O ≤ 0.5 A		–	–	0.5	–	–	0.5	

NOTE :

2– Load and line regulation are specified at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

J UA7905 • J UA7912 • J UA7915

FIXED NEGATIVE VOLTAGE REGULATORS

The UA7900M and UA7900C series are negative regulators with a fixed output voltage of −5 V, −12 V and −15 V and up to 1.5 A load current capability.

The UA7900M and UA7900C series have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limit protection against momentary faults while thermal shut down prevents junction temperature exceeding safe limits during prolonged overloads.

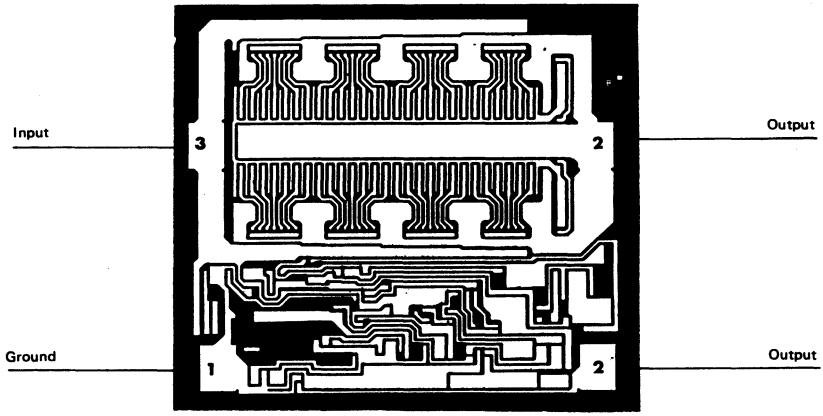
Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heatsink provided, the thermal shutdown circuit takes over preventing the IC form overheating.

These devices need only one external component : a compensation capacitor at the output, making them easy to apply.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: P964
PAD SIZE	: 0.15 x 0.20mm
DIE SIZE	: 1.89 x 1.72mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: TO39



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage J UA7915 J UA7905 - J UA7912	V_I	 −40 −35	V
Input-output voltage differential J UA7905 J UA7912/7915	$\|V_I - V_O\|$	 25 30	V
Output current	I_O	Internally limited	A
Operating junction temperature range J UA7905/12/15C J UA7905/12/15M	T_j	 0 to +125 −55 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_j = +25°C$, $V_I = -10$ V, $I_O = -0.5$ A, (Unless otherwise specified)

Characteristic	Symbol	J UA7905C			J UA7905M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range	V_O	−5.2	−5	−4.8	−5.1	−5	−4.9	V
Line regulation ($-25\ V \leq V_I \leq -7\ V$) -(Note 1)	K_{VI}	–	10	50	–	10	25	mV
Load regulation ($-5\ mA \leq I_O \leq 0.5\ A$) -(Note 1)	K_{VO}	–	30	80	–	30	80	mV
Quiescent current ($-25\ V \leq V_I \leq -7\ V$)	I_{IB}	–	2	4	–	2	4	mA
Quiescent current change ($-25\ V \leq V_I \leq -7\ V$, $-5\ mA \leq I_O \leq -0.5\ A$)	ΔI_{IB}	–	0.1	0.4	–	0.1	0.4	mA

NOTE :

1 – Load and line regulation are specified at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

ELECTRICAL OPERATING CHARACTERISTICS

$T_j = +25°C$, $V_I = -17$ V, $I_O = -0.5$ A, (Unless otherwise specified)

Characteristic	Symbol	J UA7912C			J UA7912M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range	V_O	−12.4	−12	−11.6	−12.3	−12	−11.7	V
Line regulation ($-32\ V \leq V_I \leq -14\ V$) -(Note 2)	K_{VI}	—	4	20	—	4	10	mV
Load regulation ($-5\ mA \leq I_O \leq -0.5\ A$) -(Note 2)	K_{VO}	—	30	80	—	30	80	mV
Quiescent current ($-32\ V \leq V_I \leq -14\ V$)	I_{IB}	—	2	4	—	2	4	mA
Quiescent current change ($-32\ V \leq V_I \leq -14\ V$, $-5\ mA \leq I_O \leq -0.5\ A$)	ΔI_{IB}	—	0.1	0.4	—	0.1	0.4	mA

ELECTRICAL OPERATING CHARACTERISTICS

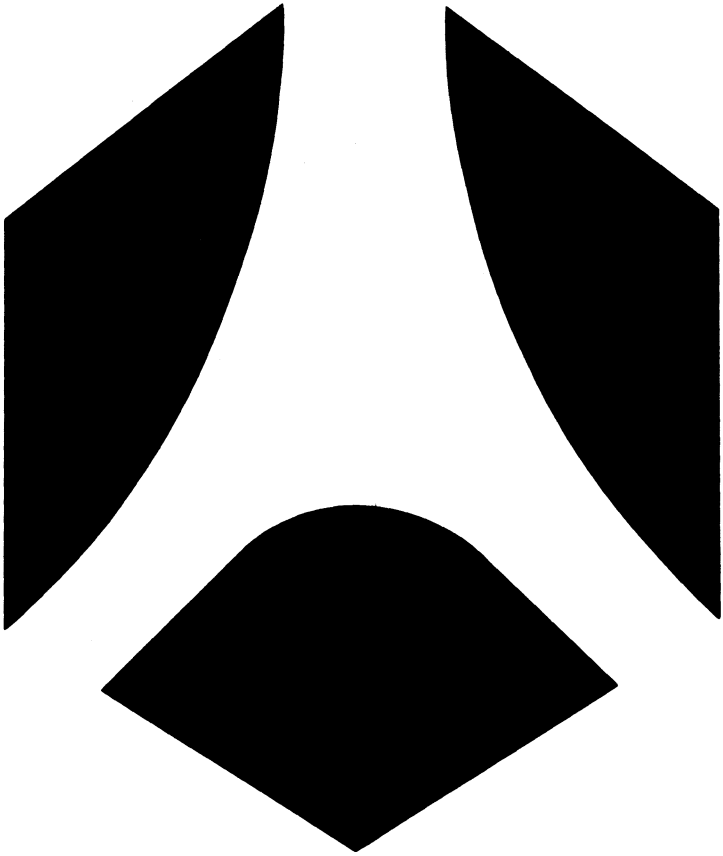
$T_j = +25°C$, $V_I = -20$ V, $I_O = -0.5$ A, (Unless otherwise specified)

Characteristic	Symbol	J UA7915C			J UA7915M			Unit
		Min	Typ	Max	Min	Typ	Max	
Output voltage range	V_O	−15.4	−15	−14.6	−15.3	−15	−14.7	V
Line regulation ($-35\ V \leq V_I \leq -17\ V$) -(Note 2)	K_{VI}	—	5	20	—	5	10	mV
Load regulation ($-5\ mA \leq I_O \leq -0.5\ A$) - (Note 2)	K_{VO}	—	30	80	—	30	80	mV
Quiescent current ($-35\ V \leq V_I \leq -17\ V$)	I_{IB}	—	2	4	—	2	4	mA
Quiescent current change ($-35\ V \leq V_I \leq -17\ V$, $-5\ mA \leq I_O \leq -0.5\ A$)	ΔI_{IB}	—	0.1	0.4	—	0.1	0.4	mA

NOTES :

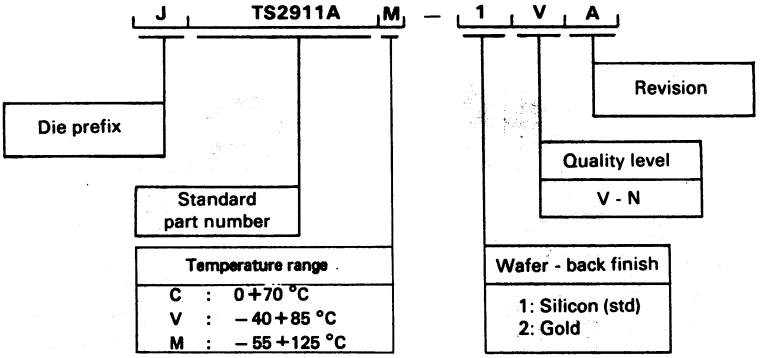
2 – Load and line regulation are specified at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.



Bipolar microprocessors & peripherals

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J TS2901B		X	X				X		A
J TS2901C		X	X				X	X	A
J TS2902A		X	X				X		A
J TS2909A		X	X				X		A
J TS2910		X	X				X		A
J TS2911A		X	X				X		A
J TS2914		X	X				X		A
J TS2915A		X	X				X		A
J TS2917A		X	X				X		A
J TS2918		X	X				X		A
J TS2919		X	X				X		A

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2901B

4-BIT MICROPROCESSOR SLICE

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the TS2901B will allow efficient emulation of almost any digital computing machine.

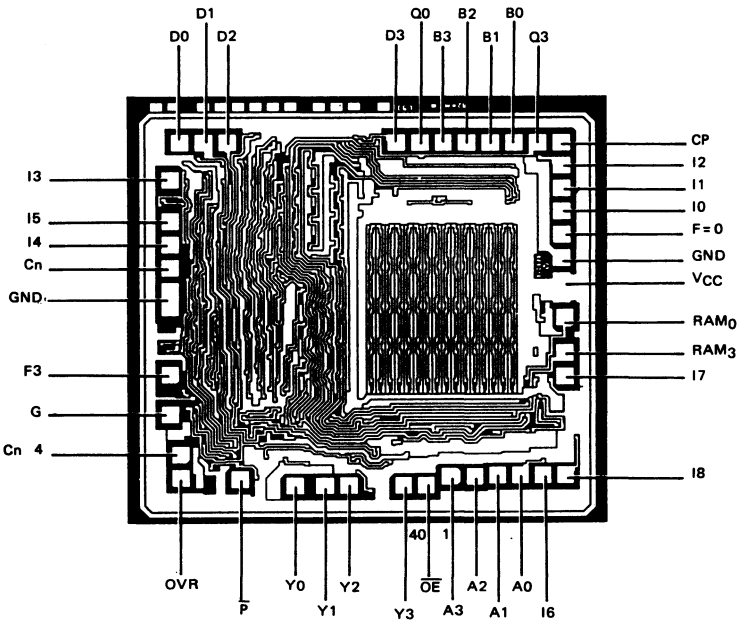
The device consists of a 16-word by 4-bit two-port RAM a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The micro-processor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this LSI chip.

- Two-address architecture
- Eight-function ALU
- Flexible data source selection
- Left/right shift independent of ALU
- Four status flags
- Expandable
- Microprogrammable

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	L931
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	3.310 x 3.015mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-182) DIL40



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_O*	1.6	W
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	+ 270	°C
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current (Note 1)		I_{CC}	180	–	240	mA
	$V_{CC} = 7.0$ V		–	–	500	
Input clamp voltage ($V_{CC} = 4.5$ V, $I_{IN} = -18$ mA)		V_{IC}	–	–	− 1	V
Low level input current ($V_{IN} = 0.5$ V)	Clock, $\overline{OE}$	I_{IL}	–	–	− 0.3	mA
	A0, A1, A2, A3, Clock		–	–	− 0.3	
	B0, B1, B2, B3		–	–	− 0.3	
	D0, D1, D2, D3		–	–	− 0.55	
	I0, I1, I2, I6, I8		–	–	− 0.3	
	I3, I4, I5, I7		–	–	− 0.55	
	$RAM_{0,3}$, $R_{0,3}$		–	–	− 0.55	
	C_n		–	–	− 0.3	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (uless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
High level Input current ($V_{IN} = 2.7$ V)	Clock, $\overline{OE}$	I_{IH}	–	–	1	µA
	A0, A1, A2, A3, Clock		–	–	1	
	B0, B1, B2, B3		–	–	1	
	D0, D1, D2, D3		–	–	1	
	I0, I1, I2, I6, I8		–	–	1	
	I3, I4, I5, I7		–	–	1	
	$RAM_{0,3}$, $Q_{0,3}$		–	–	1	
	C_n		–	–	20	
Input HIGH current ($V_{IN} = 5.5$ V)		I_I	–	–	0.02	mA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V)	$I_{OH} = -1.6$ mA; Y0, Y1, Y2, Y3	V_{OH}	2.7	–	–	V
	$I_{OH} = -1.0$ mA; C_{n+4}		2.7	–	–	
	$I_{OH} = -800$ µA; OVR, $\overline{P}$		2.7	–	–	
	$I_{OH} = -600$ µA; F3		2.7	–	–	
	$I_{OH} = -600$ µA; $RAM_{0,3}$, $Q_{0,3}$		2.7	–	–	
	$I_{OH} = -1.6$ mA; G		2.7	–	–	
Output leakage current ($V_{CC} = 4.5$ V, $V_{OH} = 5.5$ V, $V_{IN} = 2.0$ V, 0.8 V)		I_{CEX}	–	–	10	µA
Low level output voltage* ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V)	F = 0; $I_{OL} = 16$ mA	V_{OL} (I_{AV})	–	–	100	mA
	Y0, Y1, Y2, Y3; $I_{OL} = 16$ mA		–	–	100	
	$\overline{G}$; $I_{OL} = 16$ mA		–	–	100	
	C_{n+4}; $I_{OL} = 10$ mA		–	–	100	
	OVR, $\overline{P}$; $I_{OL} = 0.8$ mA		–	–	100	
	F3, $RAM_{0,3}$, $Q_{0,3}$; $I_{OL} = 6.0$ mA		–	–	100	
High impedance state output current (I_{ZH} : $V_O = 2.4$ V, I_{ZL} : $V_O = 0.5$ V)	Y0, Y1, Y2, Y3	I_{ZH}	–	–	1	µA
		I_{ZL}	–	–	– 20	
	$RAM_{0,3}$, $Q_{0,3}$	I_{ZH}	–	–	1	
		I_{ZL}	–	–	– 200	
Output short circuit current (Note 2) ($V_{CC} = 6.0$ V, $V_O = 0.5$ V)	Y0, Y1, Y2, Y3, $\overline{G}$	I_{OS}	– 30	–	– 85	mA
	C_{n+4}		– 30	–	– 85	
	OVR, $\overline{P}$		– 30	–	– 85	
	F3		– 30	–	– 85	
	$RAM_{0,3}$, $Q_{0,3}$		– 30	–	– 85	

* Measure by I_{AVAL} (note 3)

NOTES:

1– Worst case I_{CC} is at minimum temperature

2– Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

3– The I_{AVAL} measure garanties the $V_{OL} \leq 0.5$ V

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+4.5 to +5.5	V
Minimum high level input voltage	V_{IH}	+2.0	V
Maximum low level input voltage	V_{IL}	+0.8	V
Operating conditions	T_{amb}	−55 to +125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJTS2901B

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2901C

4-BIT MICROPROCESSOR SLICE

The TS2901 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the TS2901 permits efficient emulation of almost any digital computing machine.

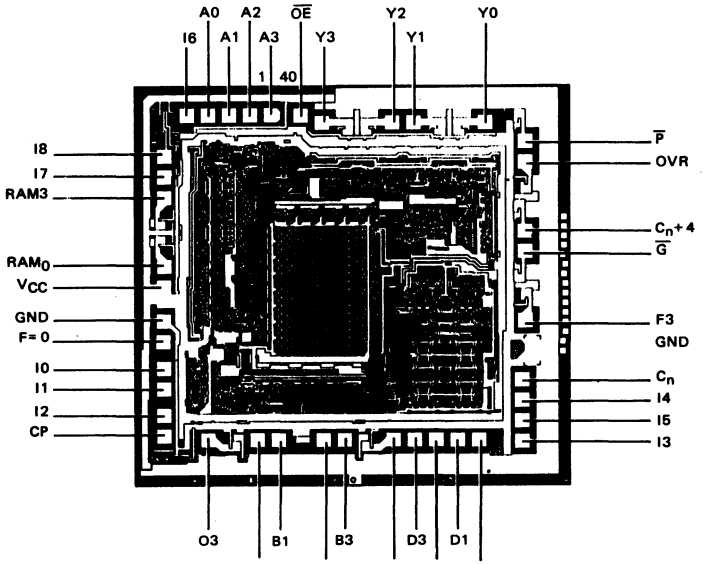
The device consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. The TS2901C is a plug-in replacement for TS2901B, but is 33 % faster than the TS2901B.

- Two-address architecture
- Eight-function ALU
- Flexible data source selection
- Left/right shift independent of ALU
- Four status flags
- Expandable
- Microprogrammable
- Fast

H BIP II

SPECIFICATIONS

PAD LAYOUT	: L971
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.12 x 3.30mm ± 0.05
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_O*	1.6	W
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, Into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	+ 270	°C
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current (Note 1)		I_{CC}	180	–	240	mA
V_{CC} = 7.0 V			–	–	500	
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA)		V_{IC}	–	–	− 1	V
Low level Input current (V_{IN} = 0.5 V)	Clock, $\overline{OE}$	I_{IL}	–	–	− 0.25	mA
	A0, A1, A2, A3, Clock		–	–	− 0.25	
	B0, B1, B2, B3		–	–	− 0.25	
	D0, D1, D2, D3		–	–	− 0.25	
	I0, I1, I2, I6, I8		–	–	− 0.25	
	I3, I4, I5, I7		–	–	− 0.25	
	$RAM_{0,3}$, $R_{0,3}$		–	–	− 0.25	
	C_n		–	–	− 0.25	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (uless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
High level input current ($V_{IN} = 2.7$ V)	Clock, $\overline{OE}$	I_{IH}	–	–	1	µA
	A0, A1, A2, A3, Clock		–	–	1	
	B0, B1, B2, B3		–	–	1	
	D0, D1, D2, D3		–	–	1	
	I0, I1, I2, I6, I8		–	–	1	
	I3, I4, I5, I7		–	–	1	
	$RAM_{0,3}$, $Q_{0,3}$		–	–	1	
	C_n		–	–	20	
Input HIGH current ($V_{IN} = 5.5$ V)		I_I	–	–	0.02	mA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V)	$I_{OH} = -1.6$ mA, Y0, Y1, Y2, Y3	V_{OH}	2.7	–	–	V
	$I_{OH} = -1.0$ mA; C_{n+4}		2.7	–	–	
	$I_{OH} = -800$ µA; OVR, $\overline{P}$		2.7	–	–	
	$I_{OH} = -600$ µA; F3		2.7	–	–	
	$I_{OH} = -600$ µA; $RAM_{0,3}$, $Q_{0,3}$		2.7	–	–	
	$I_{OH} = -1.6$ mA; $\overline{G}$		2.7	–	–	
Output leakage current ($V_{CC} = 4.5$ V, $V_{OH} = 5.5$ V, $V_{IN} = 2.0$ V, 0.8 V)		I_{CEX}	–	–	10	µA
Low level output voltage* ($V_{CC} = 4.5$ V $V_{IN} = 2.0$ V 0.8 V)	F = 0; $I_{OL} = 16$ mA	V_{OL} (I_{AV})	–	–	100	mA
	Y0, Y1, Y2, Y3; $I_{OL} = 16$ mA		–	–	100	
	$\overline{G}$; $I_{OL} = 16$ mA		–	–	100	
	C_{n+4}; $I_{OL} = 10$ mA		–	–	100	
	OVR, $\overline{P}$; $I_{OL} = 0.8$ mA		–	–	100	
	F3, $RAM_{0,3}$, $Q_{0,3}$; $I_{OL} = 6.0$ mA		–	–	100	
High impedance state output current (I_{ZH} : $V_O = 2.4$ V I_{ZL} : $V_O = 0.5$ V)	Y0, Y1, Y2, Y3	I_{ZH}	–	–	1	µA
		I_{ZL}	–	–	– 20	
	$RAM_{0,3}$, $Q_{0,3}$	I_{ZH}	–	–	1	
		I_{ZL}	–	–	– 200	
Output short circuit current (Note 2) ($V_{CC} = 6.0$ V, $V_O = 0.5$ V)	Y0, Y1, Y2, Y3, $\overline{G}$	I_{OS}	– 30	–	– 85	mA
	C_{n+4}		– 30	–	– 85	
	OVR, $\overline{P}$		– 30	–	– 85	
	F3		– 30	–	– 85	
	$RAM_{0,3}$, $Q_{0,3}$		– 30	–	– 85	

* Measure by I_{AVAL} (note 3)

NOTES:

1 – Worst case I_{CC} is at minimum temperature

2 – Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

3 – The I_{AVAL} measure garanties the $V_{OL} \leq 0.5$ V

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+4.5 to +5.5	V
Minimum high level input voltage	V_{IH}	+2.0	V
Maximum low level input voltage	V_{IL}	+0.8	V
Operating conditions	T_{amb}	−55 to +125	°C

Printed in France

Ref.DSJTS2901C

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2902A

HIGH-SPEED LOOK-AHEAD CARRY GENERATOR

The TS2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

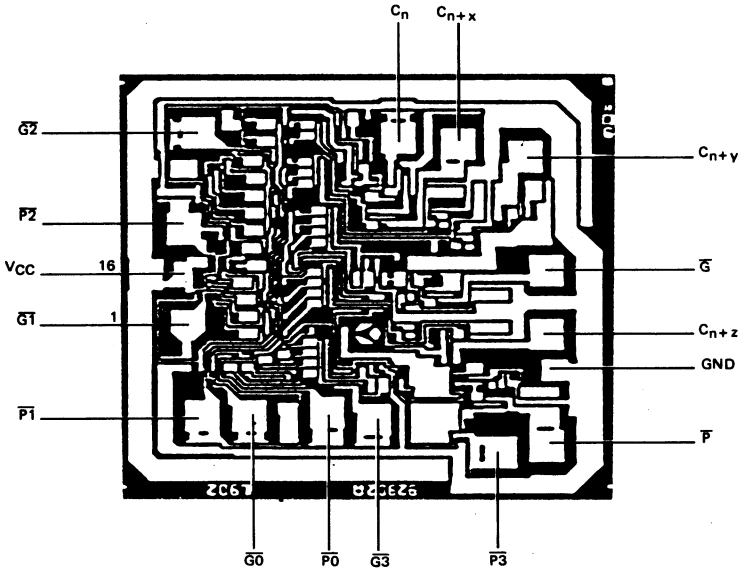
The TS2902A is generally used with the 2910 bipolar microprocessor unit to provide look-ahead over work lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

- Provides look-ahead carries accross a group of four 2901 or 2903 microprocessor ALU's.
- Capability of multi-level look-ahead for high-speed arithmetic operation over large work lengths.
- Typical carry propagation delay of 4.5 ns.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L902
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 1.575 x 1.776mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-79) DIL16



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	−	−	85	mA
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA for all inputs)		V_{IC}	−	−	− 1	V
Low level input voltage (V_{CC} = 4.5 V, I_{IN} = − 100 µA)		V_{IL}	− 420	−	− 500	mV
Low level input current (V_{IN} = 0.5 V)	C_n	I_{IL}	−	−	− 1.6	mA
	$\overline{P3}$		−	−	− 3.5	
	$\overline{P2}$		−	−	− 5.5	
	$\overline{P1}$, $\overline{G3}$, $\overline{P3}$		−	−	− 7.0	
	$\overline{G0}$, $\overline{G2}$		−	−	− 12	
	$\overline{G1}$		−	−	− 14	
High level input current (V_{IN} = 2.7 V	C_n	I_{IH}	−	−	10	µA
	$\overline{P3}$		−	−	20	
	$\overline{P2}$		−	−	40	
	$\overline{P1}$, $\overline{G3}$, $\overline{P3}$		−	−	50	
	$\overline{G0}$, $\overline{G2}$		−	−	70	
	$\overline{G1}$		−	−	70	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V *(unless otherwise specified)*

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input breakdown current (V_{IN} = 6.3 V for all inputs)	I_{NB}	–	–	125	µA
I_{AVAL} current (V_{CC} = 4.5 V, V_{AL} = 1.5 V)	I_{AV}	40	–	–	mA
High level output voltage (V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V, I_{OH} = - 1 mA)	V_{OH}	2.7	–	–	V
Output short circuit current (Note) (V_O = 0 V for all outputs)	I_{OS}	– 50	–	– 90	mA

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

The TS2909A is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two TS2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The TS2909 can select an address from any of four sources. They are:

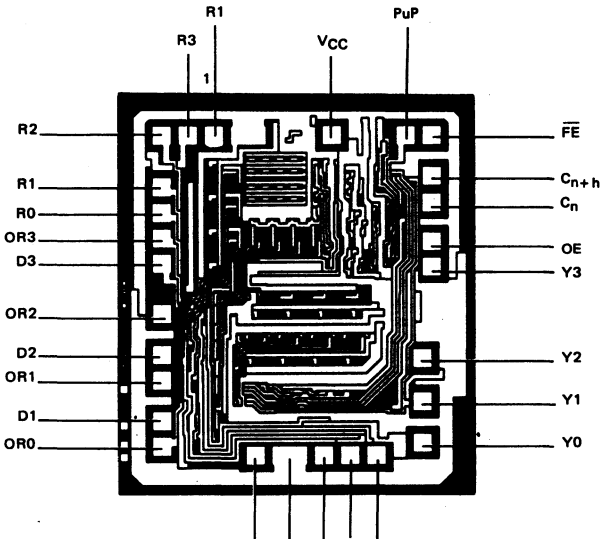
1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L932
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 2.49 x 2.21mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-132) DIL28



Back side bias : V_{CC}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, Into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	−	−	100	mA
I_{CC} low level ($V_{CC} = 0.3$ V)		I_{CO}	−	−	5	mA
Input clamp voltage ($V_{CC} = 4.5$ V, $I_{IN} = -18$ mA)		V_{IC}	−	−	− 1.2	V
Low level input current ($V_{IN} = 0.4$ V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP	I_{IL}	−	−	− 300	μA
	D0, D3		−	−	− 300	
	$\overline{OE}$, PUP		−	−	− 600	
	C_n		−	−	− 900	
High level input current ($V_{IN} = 2.7$ V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP, $\overline{OE}$	I_{IH}	−	−	2	μA
	D0, D3		−	−	4	
	C_n, PUP		−	−	4	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Input bias current ($V_{IN} = 7$ V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP, $\overline{OE}$	I_{IB}	–	–	10	µA
	D0-D3, C_n, PUP		–	–	20	
I_{AVAL} current ($V_{CC} = 4.5$ V, $V_O = 2$ V)	Y0 - Y3	I_{AV}	42	–	–	mA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V, $I_{OH} = -1$ mA)		V_{OH}	2.72	–	–	V
Output current on C_{n+4} ($V_{CC} = 4.5$ V, $V_O = 4.5$ V)		I_{CX}	–	–	250	µA
Output short circuit current (Note) ($V_{CC} = 6$ V, $V_O = 0.5$ V)	Y0 - Y3	I_{OS}	– 40	–	– 80	mA
	$C_n + 4$		– 40	–	– 80	
Output off current (I_{OZH} : $V_O = 2.4$ V, I_{OZL} : $V_O = 0.5$ V)	Y0 - Y3	I_{OZH}	–	–	2	µA
	Y0 - Y3	I_{OZL}	–	–	– 2	

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

The TS2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability ; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

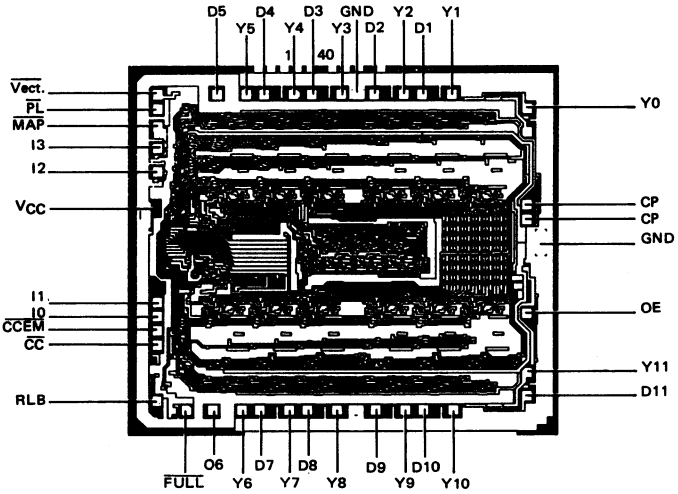
During each microinstruction, the Microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address ; 2) an external (direct) input (D) ; 3) a register/counter (R) retaining data loaded during a previous microinstruction ; or 4) a five-deep last-in, first-out stack (F).

- Twelve Bit Wide.
- Internal Loop Counter.
- Four Address Sources.
- Sixteen Powerful Microinstructions.
- Output Enable Controls for Three Branch Address Sources Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-trigerred : simplifies timing problems. Eliminates long set-up times.
- Fast Control from Condition Input : delay from condition code input to address output only 21 ns typical.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	L910
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	4.93 x 4.35mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-182) DIL40



Back side bias : V_{CC}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_O*	1.6	W
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	+ 270	°C
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	–	–	270	mA
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA)		V_{IC}	–	–	− 1.1	V
Low level input current (V_{CC} = 4.5 V, V_{IN} = 0.5 V)	D0 - D11	I_{IL}	–	–	− 0.7	mA
	CI, $\overline{CCEN}$		–	–	− 0.42	
	I0 - I3, $\overline{OE}$, $\overline{RLD}$		–	–	− 0.55	
	$\overline{CC}$		–	–	− 1.1	
	CP		–	–	− 1.7	
High level input current (V_{IN} = 2.7 V)	D0 - D11	I_{IH}	–	–	1	µA
	CI, $\overline{CCEN}$		–	–	1	
	I0 - I3, $\overline{OE}$, $\overline{RLD}$		–	–	1	
	$\overline{CC}$		–	–	5	
	CP		–	–	10	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V *(unless otherwise specified)*

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input HIGH current ($V_{IN} = 5.5$ V)	I_I	–	–	20	µA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V, $I_{OH} = -1.6$ mA)	V_{OH}	2.7	–	3.5	V
Low level output voltage * ($V_{CC} = 4.5$ V, $V_O = 1$ V)	V_{OL} (I_{AV})	20	–	–	mA
Output current ($V_O = 5.5$ V)	I_{CX}	–	–	30	µA
Output off current (I_{OZH} : $V_O = 2.4$ V, I_{OZL} : $V_O = 0.5$ V)	I_{OZH} I_{OZL}	– –	– –	1 – 1	µA
Output short circuit current (Note 1) ($V_O = 0$ V)	I_{OS}	– 40	–	– 70	mA

* Measure by I_{AVAL} (Note 2)

NOTES:

1 – Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

2 – The I_{AVAL} measure garanties the $V_{OL} \leqslant 0.5$ V.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

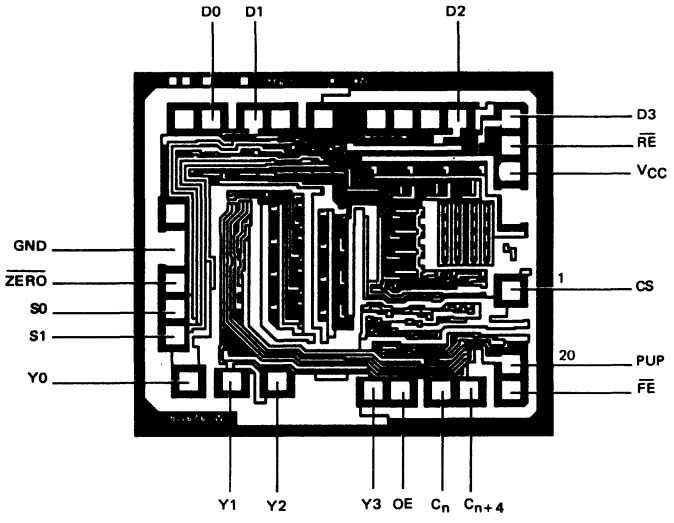
The TS2911A is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two TS2911's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	L932
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	2.49 x 2.21mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-194) DIL20



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, Into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	–	–	100	mA
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA)		V_{IC}	–	–	− 1.2	V
Low level input current (V_{IN} = 0.4 V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP	I_{IL}	–	–	− 300	μA
	D0 - D3		–	–	− 300	
	$\overline{OE}$, PUP		–	–	− 600	
	C_n		–	–	− 900	
High level input current (V_{IN} = 2.7 V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP, $\overline{OE}$	I_{IH}	–	–	2	μA
	D0 - D3		–	–	4	
	C_n, PUP		–	–	4	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Input bias current ($V_{IN} = 7$ V)	$\overline{RE}$, $\overline{ZERO}$, S0, S1, FE, CP, $\overline{OE}$	I_{IB}	–	–	10	µA
	D0-D3, C_n, PUP		–	–	20	
I_{AVAL} current ($V_{CC} = 4.5$ V, $V_O = 2$ V)	Y0 - Y3	I_{AV}	42	–	–	mA
High level ouput voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V, $I_{OH} = -1$ mA)		V_{OH}	2.72	–	–	V
Output current on $C_n + 4$ ($V_{CC} = 4.5$ V, $V_O = 4.5$ V)		I_{CX}	–	–	250	µA
Output short circuit current (Note) ($V_{CC} = 6$ V, $V_O = 0.5$ V)	Y0 - Y3	I_{OS}	– 40	–	– 80	mA
	$C_n + 4$		– 40	–	– 80	
Output off current (I_{OZH} : $V_O = 2.4$ V, I_{OZL} : $V_O = 0.5$ V)	Y0 - Y3	I_{OZH}	–	–	2	µA
	Y0 - Y3	I_{OZL}	–	–	– 2	

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2914

VECTORED PRIORITY INTERRUPT CONTROLLER

The TS2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the TS2914 makes it ideal for use in 2900 family microcomputer designs.

The TS2914 receives interrupt requests on 8 interrupt input lines (P0-P7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the TS2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins). Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

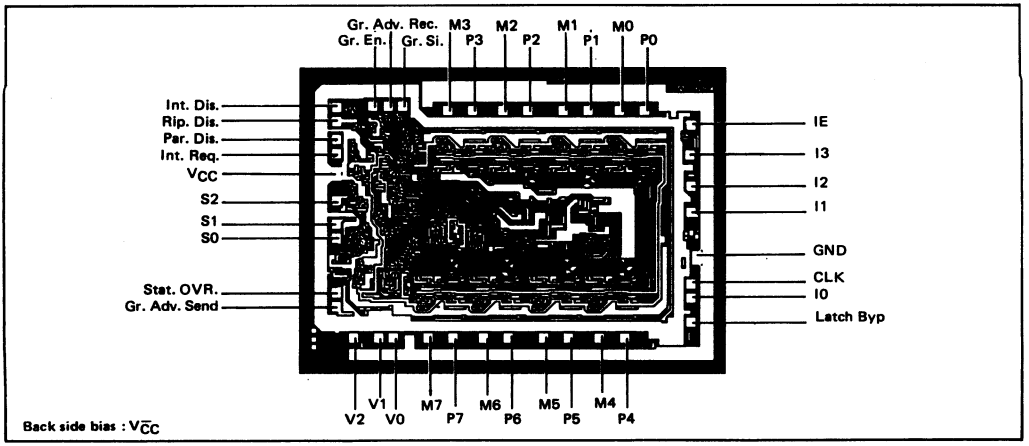
The TS2914 is controlled by a 4-bit instruction field 10-13. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

- Accepts 8 interrupt inputs
- Built-in mask register
- Built-in status register
- Vectored output
- Expandable
- Microprogrammable
- High-speed operation

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L914
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 4.90 x 3.60mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_D*	1.6	W
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	+ 270	°C
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	−	−	220	mA
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA)		V_{IC}		−	− 1.1	V
Low level input current (V_{CC} = 4.5 V), V_{IN} = 0.5 V)	P0 - P7	I_{IL}	−	−	− 0.7	mA
	$\overline{IE}$		−	−	− 0.9	
	$\overline{ID}$		−	−	− 1.5	
	LB		−	−	− 0.3	
	S0 - S2, M0 - M7		−	−	− 0.05	
High level input current (V_{IN} = 2.7 V)	P0 - P7	I_{IH}	−	−	2	µA
	$\overline{GE}$, $\overline{GAR}$		−	−	2	
	$\overline{IE}$		−	−	2	
	$\overline{ID}$		−	−	2	
	M0 - M7		−	−	10	

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Input HIGH current ($V_{IN} = 5.5$ V)		I_I	–	–	20	µA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V, $I_{OH} = 1.6$ mA)		V_{OH}	2.7	–	–	V
Low level output voltage ($V_{CC} = 4.5$ V, $I_{OL} = 12$ mA)		V_{OL}	–	–	0.46	V
Output current ($V_O = 5.5$ V)		I_{CX}	–	–	30	µA
Output off current (I_{OZH} : $V_O = 2.4$ V, I_{OZL} : $V_O = 0.5$ V)	M0 - M7	I_{OZH}	–	–	20	µA
	S0 - S2		–	–	20	
	V0 - V2		–	–	10	
	M0 - M7	I_{OZL}	–	–	– 20	
	S0 - S2		–	–	– 20	
	V0 - V2		–	–	– 10	
Output short circuit current (Note) ($V_O = 0$ V)		I_{OS}	– 40	–	– 70	mA

NOTE:
Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2915A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The TS2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

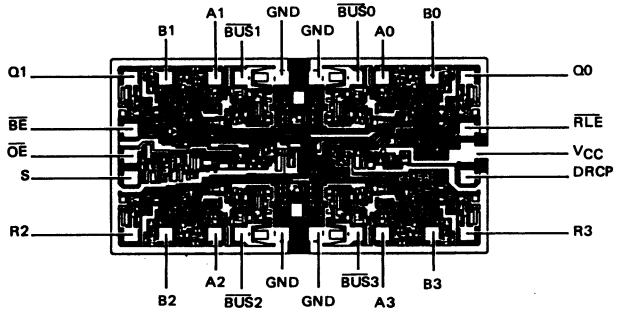
Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs ($\overline{BUS}$ data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48 mA at 0.5 V max
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 3.5 V minimum output high voltage for direct interface to MOS microprocessors.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L915
PAD SIZE	: 0.1 x 0 1mm
DIE SIZE	: 3.44 x 2.02mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-68) DIL24



Back side bias : V_{CC}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_O*	1.6	W
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	+ 270	°C
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	−	−	100	mA
Input clamp voltage (V_{CC} = 4.5 V except bus, I_{IN} = − 18 mA)		V_{IC}	− 1	−	−	V
Low level input current (V_{CC} = 5.5 V except bus, V_{IN} = 0.4 V)	$\overline{BE}$, $\overline{RLE}$ Other inputs	I_{IL}	− −	− −	− 0.6 − 0.3	mA
High level input current (V_{CC} = 5.5 except bus, V_{IN} = 2.7 V)		I_{IH}	−	−	1	µA
Input HIGH current (V_{CC} = 5.5 V except bus, V_{IN} = 7 V)		I_I	−	−	1	µA
High level output voltage (V_{CC} = 4.5 V, V_{IN} = 2.0, 0.8 V)	I_{OH} = − 15 mA, $\overline{BUS}_{0\text{-}3}$ I_{OH} = − 1.0 mA, RCVR output	V_{OH}	2.7 2.7	− −	− −	V
Low level output voltage (V_{CC} = 4.5 V V_{IN} = 2.0 V, 0.8 V)	I_{OL} = 48 mA, $\overline{BUS}_{0\text{-}3}$ I_{OL} = 12 mA, RCVR output	V_{OL}	− −	− −	0.48 0.45	V

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
V_{OUT} Receiver ($V_{CC} = 5$ V, $I_{OFR} = -100\ \mu A$)		V_{OFR}	–	–	3.7	V
Bus leakage current	$V_{OUT} = 0.4$ V $V_{OUT} = 2.4$ V $V_{OUT} = 4.5$ V	I_O	– – –	– – –	– 70 20 20	µA
Bus leakage current power off ($V_{CC} = 0$ V, $V_{OUT} = 4.5$ V)		I_{OFF}	–	–	50	µA
Off state output current ($V_{CC} = 5.5$ V except bus)	$V_{OUT} = 0.4$ V $V_{OUT} = 2.4$ V	I_O	– –	– –	– 20 20	µA
Output short circuit current (Note)	$\overline{BUS}_{0\text{-}3}$ RCVR output	I_{OS}	– 70 – 40	– –	– 200 – 100	mA

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2917A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

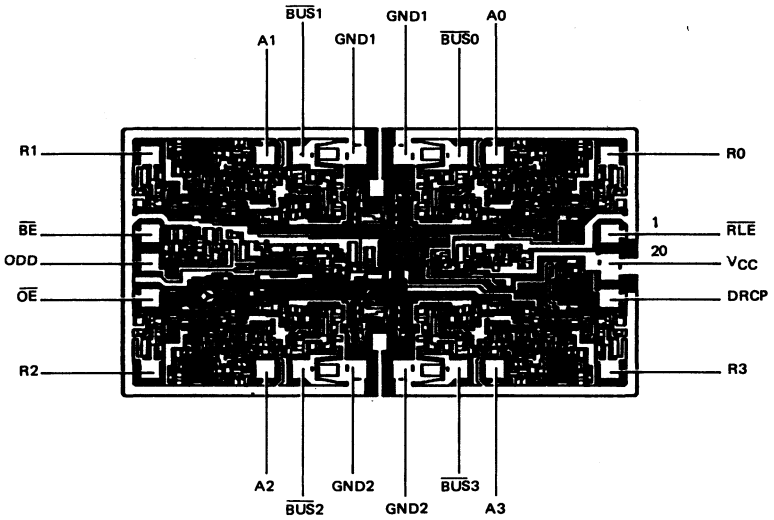
The TS2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48 mA at 0.5 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 3.5 V minimum output high voltage for direct interface to MOS microprocessors.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	:	L917
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	3.44 x 2.02mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-194) DIL20



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power supply current		I_{CC}	5	–	75	mA
Input clamp voltage (V_{CC} = 4.5 V except bus, I_{IN} = − 18 mA)		V_{IC}	− 1	–	–	V
Low level input current (V_{CC} = 5.5 V except bus, V_{IN} = 0.4 V)	$\overline{BE}$, $\overline{RLE}$ Other inputs	I_{IL}	– –	– –	− 0.6 − 0.3	mA
High level input current (V_{CC} = 5.5 V except bus, V_{IN} = 2.7 V)		I_{IH}	–	–	1	µA
Input HIGH current (V_{CC} = 5.5 V except bus, V_{IN} = 7 V)		I_I	–	–	1	µA
High level output voltage (V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V)	I_{OH} = 15 mA, $\overline{BUS}$ 0.3 I_{OH} = 1.0 mA, RCVR output I_{OH} = 100 µA, RCVR output I_{OH} = 660 µA, Parity output	V_{OH}	2.7 2.7 3.8 2.7	– – – –	– – – –	V

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min	Typ.	Max.	Unit
Bus leakage current	V_{OUT} = 0.4 V V_{OUT} = 2.4 V V_{OUT} = 4.5 V	I_O	– – –	– – –	– 70 20 20	µA
Off state output current (V_{CC} = 5.5 V except bus)	V_{OUT} = 0.4 V V_{OUT} = 2.4 V	I_O	– –	– –	– 20 20	µA
Output short circuit current (Note)	$\overline{BUS}_{0-3}$ RCVR output Parity output	I_{OS}	– 70 – 40 – 30	– – –	– 200 – 100 – 80	mA

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2918

QUAD D REGISTER WITH STANDARD AND THREE-STATE OUTPUTS

New Schottky circuits such as the TS2918 register provide the design engineer with additional flexibility in system configuration – especially with regard to bus structure, organization and speed. The TS2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

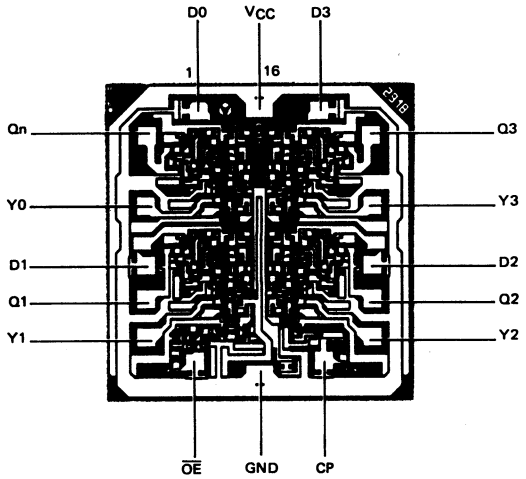
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The TS2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the TS2918 register. Other applications of TS2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency.

BIPOLAR

PAD LAYOUT	:	L918
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	2.01 x 1.96mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-79) DIL16



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Maximum power dissipation	P_O*	1.6	W
Voltage applied to outputs for HIGH Outputs state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, Into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

* Must with stand the added P_O due to short circuit test.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Power supply current	I_{CC}	–	–	130	mA
Input clamp voltage (V_{CC} = 4.5 V, I_{IN} = − 18 mA)	V_{IC}	–	–	− 1.2	V
Low level Input current (Note 1) (V_{IN} = 0.5 V)	I_{IL}	–	–	− 2	mA
High level Input current (Note 1) (V_{IN} = 2.7 V)	I_{IH}	–	–	50	µA
Input HIGH current (V_{IN} = 5.5 V)	I_I	–	–	1	mA
High level output voltage (V_{CC} = 4.5 V, V_{IN} = 2.0, 0.8 V) I_{OH} = − 2 mA, Y0 - Y3 I_{OH} = − 1 mA, Q0 - Q3	VOH	2.4 2.7	– –	– –	V
Low level output voltage (V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V, I_{OL} = 20 mA	V_{OL}	–	–	0.5	V

ELECTRICAL OPERAT'NG CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 5.5 V (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Off state output current (V_{OUT} = 0.4 V (V_{CC} = 4.5 V) V_{OUT} = 2.4 V	I_O	– –	– –	– 20 20	µA
Output short circuit current (Note 2) (V_{OUT} = 0 V)	I_{OS}	– 40	–	– 100	mA

NOTES:

1– Actual input current = Unit load current x input load factor.

2– Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS2919

QUAD REGISTER WITH DUAL THREE-STATE OUTPUTS

The TS2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

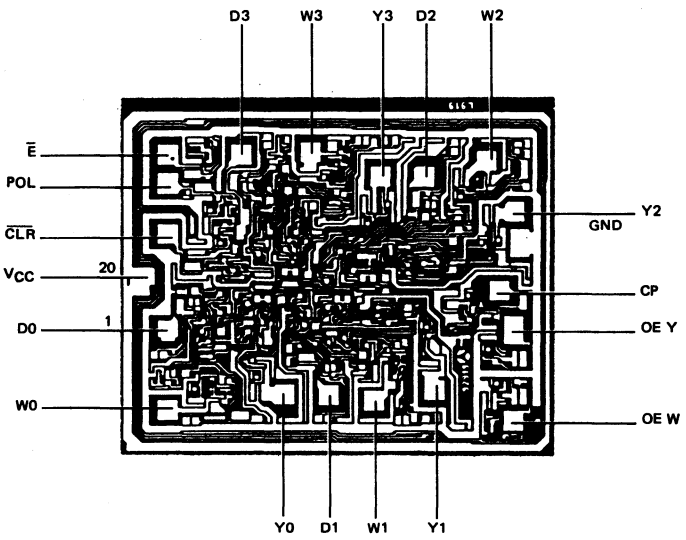
The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The TS2919 is packaged in a space-saving 20-pin package.

- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs.

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L919
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 2.515 x 2.108mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-194) DIL20



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage to ground potential	V_{CC}	− 0.5 to + 7.0	V
Voltage applied to Outputs for HIGH output state		− 0.5 to V_{CC} max.	V
Input voltage range	V_{IN}	− 0.5 to + 5.5	V
Output current, Into Outputs	I_O	+ 30	mA
Input current	I_I	− 30 to + 5.0	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	+ 175	°C
Ambient temperature under Bias	T_{amb}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Power supply current	I_{CC}	−	−	36	mA
Input clamp voltage ($V_{CC} = 4.5$ V, $I_{IN} = -18$ mA)	V_{IC}	−	−	− 1.5	V
Low level Input current ($V_{IN} = 0.4$ V)	I_{IL}	−	−	− 0.36	mA
High level Input current ($V_{IN} = 2.7$ V)	I_{IH}	−	−	20	µA
Input HIGH current ($V_{IN} = 7$ V)	I_I	−	−	0.1	mA
High level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$, 0.8 V, $I_{OH} = -1$ mA)	V_{OH}	−	−	2.4	V

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 5.5$ V (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Low level output voltage ($V_{CC} = 4.5$ V, $V_{IN} = 2.0$ V, 0.8 V)	I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA	V_{OL}	– – –	– – –	0.4 0.45 0.5	V
Off state output current	V_{OUT} = 0.4 V V_{OUT} = 2.4 V	I_{OFF}	– –	– –	– 20 20	µA
Output short circuit current (Note) (V_{OUT} = 0 V)		I_{OS}	– 15	–	– 85	mA

NOTE:

Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Operating conditions	T_{amb}	– 55 to + 125	°C

These specifications are subjet to change without notice.
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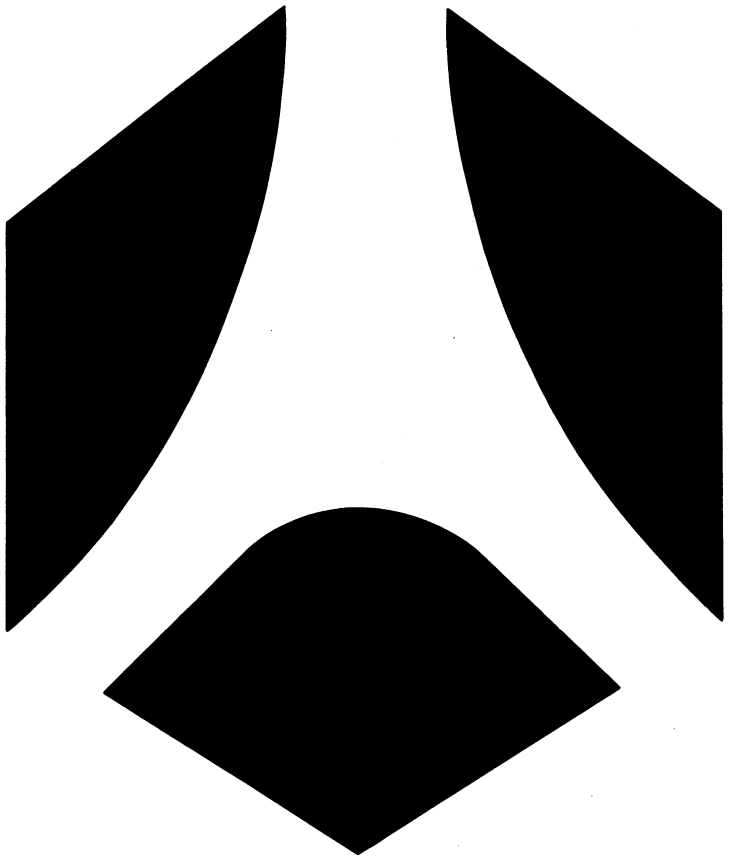
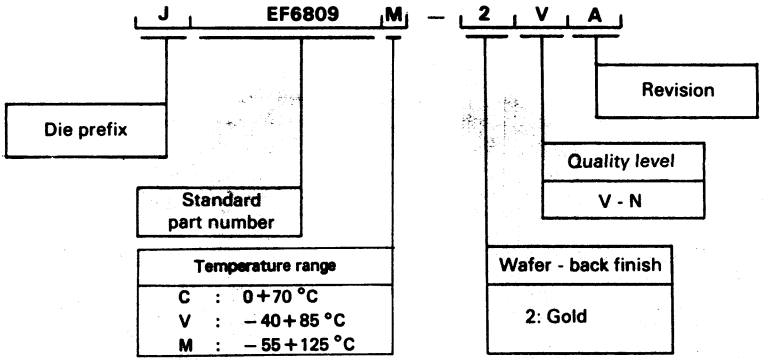


6800 microprocessors & peripherals

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J EF6800		X	X					X	A
J EF6802		X	X					X	A
J EF6803		X	X					X	A
J EF68HC05E2		X	X					X	A
J EF6809		X	X					X	A
J EF6809E		X	X					X	A
J EF6810		X	X					X	A
J EF6821		X	X					X	A
J EF6840		X	X					X	A
J EF6850		X	X					X	A
J EF6852		X	X					X	A
J EF6854		X	X					X	A

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6800

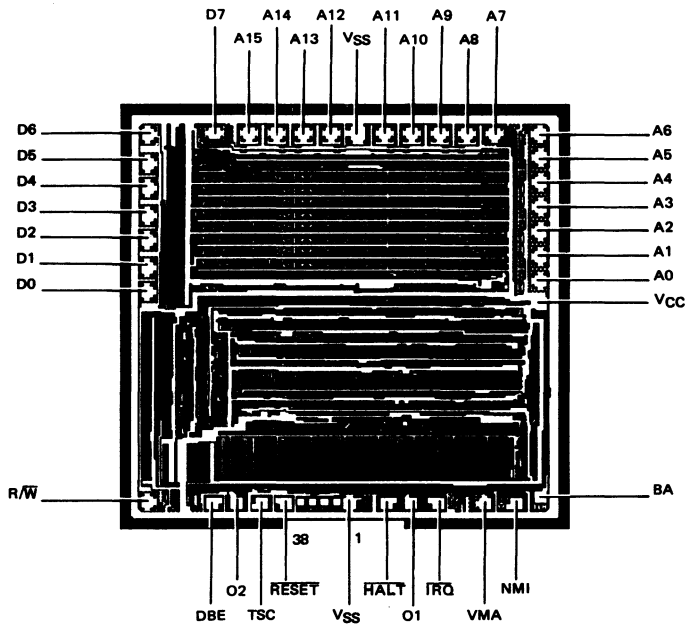
8-BIT MICROPROCESSOR UNIT (MPU)

The EF6800 is a monolithic 8-bit microprocessor forming the central control function for THOMSON SEMICONDUCTEURS' 6800 family. Compatible with TTL, the EF6800, as with all 6800 system parts, requires only one + 5.0 V power supply, and no external TTL devices for bus interface.
The EF6800 is capable of addressing 64K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as three-state, making direct memory addressing and multiprocessing applications realizable.

NMOS

SPECIFICATIONS

PAD LAYOUT	:	609.2
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	3.92 x 4.00mm ± 0.05
DIE THICKNESS	:	0.375mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	(CB-182) DIL40



Back side bias : V_{SS}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc, ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic	V_{IH}	V_{SS} + 2.0	–	–	V
	$\phi1, \phi2$	V_{IHC}	V_{CC} − 0.6	–	–	
Input Low Voltage	Logic	V_{IL}	–	–	V_{SS} + 0.8	V
	$\phi1, \phi2$	V_{ILC}	–	–	V_{SS} + 0.4	
Input Leakage Current						
(V_{in} = 0 to 5.25 V, V_{CC} = Max)	Logic	I_{in}	–	1.0	2.5	μA
(V_{in} = 0 to 5.25 V, V_{CC} = 0 V to 5.25 V)	$\phi1, \phi2$		–	–	100	
Hi-Z Input Leakage Current	D0-D7	I_{TZ}	–	2.0	10	μA
(V_{in} = 0.4 to 2.4 V, V_{CC} = Max)	A0-A15, R/$\overline{W}$		–	–	100	
Output High Voltage						
(I_{Load} = − 205 μA, V_{CC} = Min)	D0-D7	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = − 145 μA, V_{CC} = Min)	A0-A15, R/$\overline{W}$, VMA		V_{SS} + 2.4	–	–	
(I_{Load} = − 100 μA, V_{CC} = Min)	BA		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mA, V_{CC} = Min)		V_{OL}	–	–	V_{SS} + 0.4	V
Internal Power Dissipation (Measured at $T_{amb} = T_L$)		P_{INT}	–	0.5	1.0	W
Capacitance						
(V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	$\phi1$		–	25	–	
	$\phi2$	C_{in}	–	45	–	pF
	D0-D7		–	10	–	
	Logic Inputs		–	6.5	–	
	A0-A15, R/$\overline{W}$, VMA	C_{out}	–	–	–	pF

CLOCK TIMING (V_{CC} = 5.0 V, ± 5%, V_{SS} = 0, T_{amb} = T_L to T_H unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency of Operation			0.1	–	1.0	MHz
Cycle Time			1.000	–	10	µs
Clock Pulse Width (Measured at V_{CC} – 0.6 V)	ϕ1, ϕ2		400	–	9500	ns
Delay Time or Clock Separation (Measured at $V_{OV} = V_{SS} + 0.6$ V @ $t_r = t_f \leq 100$ ns) (Measured at $V_{OV} = V_{SS} + 1.0$ V @ $t_r = t_f \leq 35$ ns)		t_d	0 0	– –	9100 9100	ns

READ/WRITE TIMING

Characteristic	Symbol	J EF6800			Unit
		Min	Typ	Max	
Address Delay C = 90 pF C = 30 pF	t_{AD}	– –	– –	270 250	ns
Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	605	–	–	ns
Data Setup Time (Read)	t_{DSR}	100	–	–	ns
Input Data Hold Time	t_H	10	–	–	ns
Output Data Hold Time *	t_H	10	25	–	ns
Address Hold Time (Address, R/W, VMA) *	t_{AH}	10	50	–	ns
Enable High Time for DBE Input	t_{EH}	450	–	–	ns
Data Delay Time (Write)	t_{DDW}	–	–	225	ns
Processor Controls Processor Control Setup Time Processor Control Rise and Fall Time Bus Available Delay Hi-Z Enable Hi-Z Delay Data Bus Enable Down Time During ϕ1 Up Time Data Bus Enable Rise and Fall Times	 t_{PCS} t_{PCr}, t_{PCf} t_{BA} t_{TSE} t_{TSD} t_{DBE} t_{DBEr}, t_{DBEf}	 200 – – 0 – 150 –	 – – – – – – –	 – 100 250 40 270 – 25	 ns

* Not tested

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6802

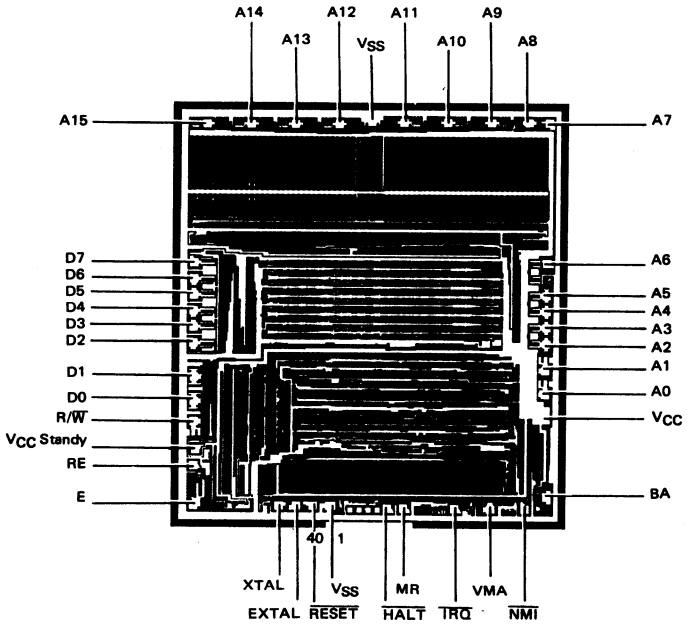
MICROPROCESSOR WITH CLOCK AND OPTIONAL RAM

The EF6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present EF6800 plus an internal clock oscillator and driver on the same chip. In addition, the EF6802 has 128 bytes of on-board RAM located at hex addresses $0000 to $007F. The first 32 bytes of RAM, at hex addresses $0000 to $001F, may be retained in a low power mode by utilizing V_{CC} standby ; thus, facilitating memory retention during a power-down situation.
The EF6802 is completely software compatible with the EF6800 as well as the entire EF6800 family of parts. Hence, the EF6802 is expandable to 64K words.

NMOS

SPECIFICATIONS

PAD LAYOUT	: 608.3
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 4.76 x 5.64mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : V_{SS}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	− 55 to + 125	°C
Storage Temperature Range	T_{stg}	− 55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, EXTAL RESET	V_{IH}	V_{SS} + 2.0 V_{SS} + 4.0	– –	– –	V
Input Low Voltage	Logic, EXTAL, RESET	V_{IL}	–	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic	I_{in}	–	1.0	2.5	µA
Output High Voltage (I_{Load} = − 205 µA, V_{CC} = min) (I_{Load} = − 145 µA, V_{CC} = min) (I_{Load} = − 100 µA, V_{CC} = min)	 D0-D7 A0-A15, R/W, VMA, E BA	V_{OH}	 V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	 – – –	 – – –	V
Output Low Voltage (I_{Load} = 1.6 mA, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	V
Internal Power Dissipation (Measured at T_{amb} = 0°C)		P_{INT}	–	0.750	1.0	W
V_{CC} Standby	Power Down Power Up	V_{SBB} V_{SB}	4.0 4.75	– –	5.25 5.25	V
Standby Current		I_{SBB}	–	–	8.0	mA
Capacitance * (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	D0-D7 Logic Inputs, EXTAL	C_{in}	– –	10 6.5	12.5 10	pF
	A0-A15, R/W, VMA	C_{out}	–	–	12	pF

* Not tested

CONTROL TIMING (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristics	Symbol	J EF6802		Unit
		Min	Max	
Frequency of Operation	f_o	0.1	1.0	MHz
Crystal Frequency	f_{XTAL}	1.0	4.0	MHz
External Oscillator Frequency	$4xf_o$	0.4	4.0	MHz
Crystal Oscillator Start Up Time	t_{rc}	100	–	ms
Processor Controls (HALT, MR, RE, RESET, IRQ NMI) Processor Control Setup Time Processor Control Rise and Fall Time (Does Not Apply to RESET)	 t_{PCS} t_{PCr}, t_{PCf}	 200 –	 – 100	 ns ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS.JEF6802

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6803

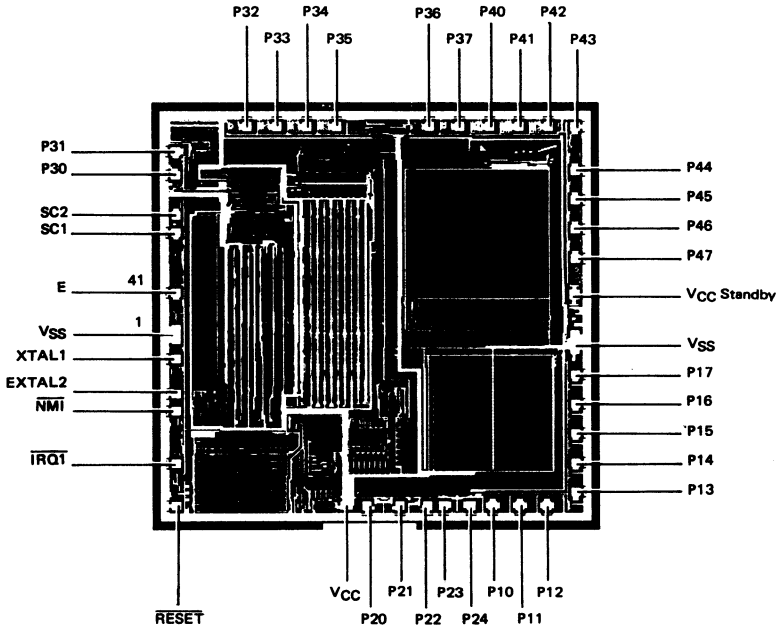
MICROCOMPUTER/MICROPROCESSOR (MCU/PMU)

The EF6801 is an 8-bit single-chip microcomputer unit (MCU) which significantly enhances the capabilities of the 6800 family of parts. It includes an upgraded 6800 microprocessor unit (MPU) with upward-source and object-code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned multiply. The MCU can function as a monolithic microcomputer or can be expanded to a 64K byte address space. It is TTL compatible and requires one + 5-volt power supply. On-chip resources include 2048 bytes of ROM, 128 bytes of RAM, a Serial Communications Interface (SCI), parallel I/O, and a three function Programmable Timer. The EF6803 can be considered as an EF6801 operating in Modes 2 or 3.

HMOS

SPECIFICATIONS

PAD LAYOUT	: OFB.1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.34 x 5.20mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxyde
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL 40



Back side bias : V_{SS}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range EF6803	T_{amb}	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	EF6803 Min	EF6803 Max	Unit
Input High Voltage	$\overline{RESET}$	V_{IH}	V_{SS} + 4.0	V_{CC}	V
	Other Inputs		V_{SS} + 2.0	V_{CC}	
Input Low Voltage	All Inputs	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Load Current	Port 4	I_{in}	–	0.5	mA
(V_{in} = 0 to 2.4 V)	SCI		–	0.8	
Input Leakage Current (V_{in} = 0 to 5.25 V)	$\overline{NMI}$, $\overline{IRQ1}$, $\overline{RESET}$	I_{in}	–	2.5	µA
Hi-Z (Off State) Input Current (V_{in} = 0.5 to 2.4 V)	Ports 1, 2, and 3	I_{TSI}	–	10	µA
Output High Voltage (I_{Load} = − 65 µA, V_{CC} = Min)*	E, Port 4, SC1, SC2	V_{OH}	V_{SS} + 2.4	–	V
(I_{Load} = − 100 µA, V_{CC} = Min)	Other Outputs		V_{SS} + 2.4	–	
Output Low Voltage (I_{Load} = 2.0 mA, V_{CC} = Min)	All Outputs	V_{OL}	–	V_{SS} + 0.5	V
Darlington Drive Current (V_O = 1.5 V)	Port 1	I_{OH}	1.0	4.0	mA
Internal Power Dissipation (Measured at T_{amb} = T_L in Steady-State Operation)		P_{INT}	–	1200	mW
Input Capacitance	Port 3, Port 4, SCI	C_{in}	–	12.5	pF
(V_{in} = 0, T_{amb} = 25°C, f_o = 1.0 MHz)	Other Inputs		–	10	
V_{CC} Standby	Powerdown	V_{SBB}	4.0	5.25	V
	Powerup	V_{SB}	4.75	5.25	
Standby Current	Powerdown	I_{SBB}	–	6.0	mA

* Negotiable to − 100 µA (for further information contact the factory)

CONTROL TIMING (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	EF6803 Min	EF6803 Max	Unit
Frequency of Operation	f_o	0.5	1.0	MHz
Crystal Frequency	f_{XTAL}	2.0	4.0	MHz
External Oscillator Frequency	$4f_o$	2.0	4.0	MHz
Crystal Oscillator Start Up Time	t_{rc}	–	100	ms
Processor Control Setup Time	t_{PCS}	200	–	ns

PERIPHERAL PORT TIMING

Characteristics	Symbol	EF6803 Min	EF6803 Max	Unit
Peripheral Data Setup Time	t_{PDSU}	200	–	ns
Peripheral Data Hold Time	t_{PDH}	200	–	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Negative Transition	t_{OSD1}	–	350	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Positive Transition	t_{OSD2}	–	350	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid	t_{PWD}	–	350	ns
Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid	t_{CMOS}	–	2.0	µs
Input Strobe Pulse Width	t_{PWIS}	200	–	ns
Input Data Hold Time	t_{IH}	50	–	ns
Input Data Setup Time	t_{IS}	20	–	ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

THOMSON COMPONENTS SEMICONDUCTEURS

J EF68HC05E2

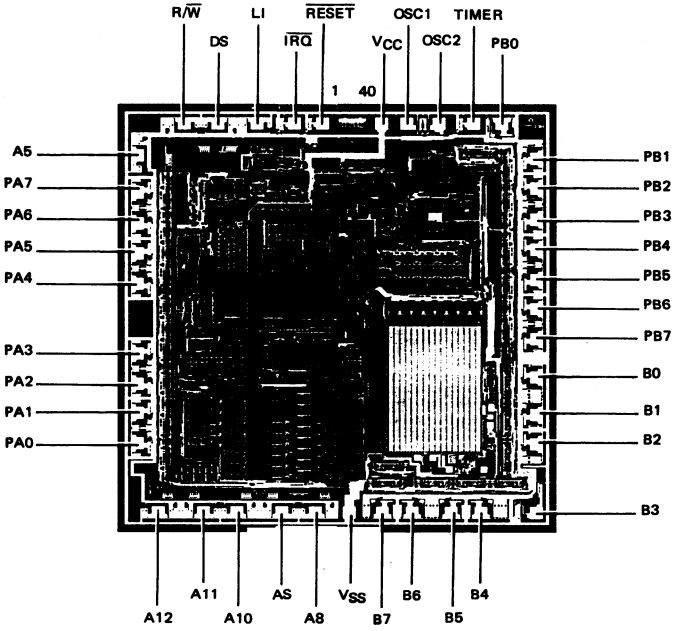
8-BIT MICROPROCESSOR UNIT (MPU)

The EF68HC05E2 Microprocessor Unit (MPU) belongs to the EF6805 Family of Microcomputers. This 8-bit fully static and expandable microprocessor contains a CPU, on-chip RAM, I/O, and TIMER. It is a low-power, low-cost processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor.

HCMOS

SPECIFICATIONS

PAD LAYOUT	: OGW.1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.50 x 5.46mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : V_{SS}

April 1987-1/4

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MAXIMUM RATINGS (voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8.0	V
All Input Voltages Except OSC1	V_{in}	V_{SS}-0.5 to V_{DD}+0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_{amb}	- 55 to + 125	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS @ 5.0 V (V_{DD}= 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Max	Unit
Output Voltage ($I_{Load} \leq 10.0\ \mu A$)	V_{OL} V_{OH}	– $V_{DD}-0.1$	0.1 –	V
Total Supply Current (C_L = 130 pF – On Bus, C_L = 50 pF – On Ports, No dc Loads, t_{cyc} = 1.0 µs, V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V)	I_{DD}			
Run		–	10	mA
Wait (Test Conditions – See Note 1)		–	1.5	mA
Stop (Test Conditions – See Note 1)		–	200	µA
Output High Voltage	V_{OH}			V
(I_{Load} = 1.6 mA) A8-A12, B0-B7, DS, AS, R/$\overline{W}$		4.1	–	
(I_{Load} = 0.36 mA) PA0-PA7, PB0-PB7		4.1	–	
Output Low Voltage (I_{Load} = 1.6 mA) A8-A12, B0-B7, PA0-PA7, PB0-PB7, DS, AS, R/$\overline{W}$	V_{OL}	–	0.4	V
Input High Voltage	V_{IH}			V
PA0-PA7, PB0-PB7, B0-B7		$V_{DD}-2.0$	–	
TIMER, $\overline{IRQ}$, $\overline{RESET}$		$V_{DD}-0.8$	–	
OSC1		$V_{DD}-1.5$	–	
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation	f_{osc}			MHz
Crystal		–	5.0	
External Clock		dc	5.0	
Input Current $\overline{RESET}$, $\overline{IRQ}$, TIMER, OSC1	I_{in}	–	± 1	µA
Hi-Z Output Leakage Current PA0-PA7, PB0-PB7, B0-B7	I_{TSI}	–	± 10	µA
Capacitance * $\overline{RESET}$, $\overline{IRQ}$, TIMER	C_{in}	–	8.0	pF
Capacitance * DS, AS, R/$\overline{W}$, A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12.0	pF

NOTE: 1-Test conditions for Quiescent Current Values are:
Port A and B programmed as inputs.
V_{IL} = 0.2 V for PA0-PA7, PB0-PB7, and B0-B7.
V_{IH} = V_{DD} – 0.2 V for $\overline{RESET}$, $\overline{IRQ}$, and TIMER.
OSC1 input is a squarewave from V_{SS} + 0.2 V to V_{DD} – 0.2 V.
OSC2 output load (including tester) is 35 pF maximum.
Wait mode (I_{DD}) is affected linearly by this capacitance.

* Not tested

ELECTRICAL OPERATING CHARACTERISTICS @ 3.0 V (V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Max	Unit
Output Voltage ($I_{Load} \leq 10.0\ \mu A$)	V_{OL} V_{OH}	– $V_{DD}-0.1$	0.1 –	V
Total Supply Current (C_L = 50 pF – No dc Loads, t_{cyc} = 5 µs)	I_{DD}			
Run (V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V)		–	1.3	mA
Wait (Test Conditions – See Note 1)		–	200	µA
Stop (Test Conditions – See Note 1)		–	100	µA
Output High Voltage	V_{OH}			V
(I_{Load} = 0.25 mA) A8-A12, B0-B7, DS, AS, R/$\overline{W}$		2.7	–	
(I_{Load} = 0.1 mA) PA0-PA7, PB0-PB7		2.7	–	
Output Low Voltage				
(I_{Load} = 0.25 mA) A8-A12, B0-B7, PB0-PB7, DS, AS, R/$\overline{W}$, PA0-PA7	V_{OL}	–	0.3	V
Input High Voltage	V_{IH}			V
PA0-PA7, PB0-PB7, B0-B7		2.1	–	
TIMER, $\overline{IRQ}$, $\overline{RESET}$		2.5	–	
OSC1		2.1	–	
Input Low Voltage (All Inputs)	V_{IL}	–	0.5	V
Frequency of Operation	f_{osc}			MHz
Crystal		–	1.0	
External Clock		dc	1.0	
Input Current				
$\overline{RESET}$, $\overline{IRQ}$, TIMER, OSC1	I_{in}	–	± 1	µA
Hi-Z Output Leakage Current				
PA0-PA7, PB0-PB7, B0-B7	I_{TSL}	–	± 10	µA
Capacitance				
$\overline{RESET}$, $\overline{IRQ}$, TIMER	C_{in}	–	8.0	pF
Capacitance				
DS, AS, R/$\overline{W}$, A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12.0	pF

NOTE: 1 - Test conditions for Quiescent Current Values are:
Port A and B programmed as inputs.
V_{IL} = 0.2 V for PA0-PA7, PB0-PB7, and B0-B7.
$V_{IH} = V_{DD} - 0.2$ V for $\overline{RESET}$, $\overline{IRQ}$, and TIMER
OSC1 input is a squarewave from V_{SS} + 0.2 V to V_{DD} – 0.2 V.
OSC2 output load (including tester) is 35 pF maximum.
Wait mode I_{DD} is affected linearly by this capacitance.

CONTROL TIMING (V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

		V_{DD} = 3.0 V f_{osc} = 1 MHz			V_{DD} = 5.0 V ± 10% f_{osc} = 5.0 MHz			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
I/O Port Timing – Input Setup Time	t_{PVASL}	500	–	–	250	–	–	ns
Input Hold Time	t_{ASLPX}	100	–	–	100	–	–	ns
Output Delay Time	t_{ASLPV}	–	–	0	–	–	0	ns
Interrupt Setup Time	t_{ILASL}	2	–	–	0.4	–	–	µs
Crystal Oscillator Startup Time	t_{OXOV}	–	30	300	–	15	100	ms
Wait Recovery Startup Time	t_{IVASH}	–	–	10	–	–	2	µs
Stop Recovery Startup Time (Crystal Oscillator)	t_{ILASH}	–	30	300	–	15	100	ms
Required Interrupt Release	t_{DSLIH}	–	–	5	–	–	1.0	µs
Timer Pulse Width	t_{TH}, t_{TL}	0.5	–	–	0.5	–	–	t_{cyc}
Reset Pulse Width	t_{RL}	5.5	–	–	1.5	–	–	µs
Timer Period	t_{TLTL}	1.0	–	–	1.0	–	–	t_{cyc}
Interrupt Pulse Width Low	t_{ILIH}	1.0	–	–	1.0	–	–	t_{cyc}
Interrupt Pulse Period	t_{ILIL}	*	–	–	*	–	–	t_{cyc}
Oscillator Cycle Period (1/5 of t_{cyc})	t_{OLOL}	1000	–	–	200	–	–	ns
OSC1 Pulse Width High	t_{OH}	350	–	–	75	–	–	ns
OSC1 Pulse Width Low	t_{OL}	350	–	–	75	–	–	ns

* The minimum period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.

These specifications are subjet to change without notice.
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Ref.DSJEF68HC05E2

The EF6809 is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the 6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The EF6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

The EF6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

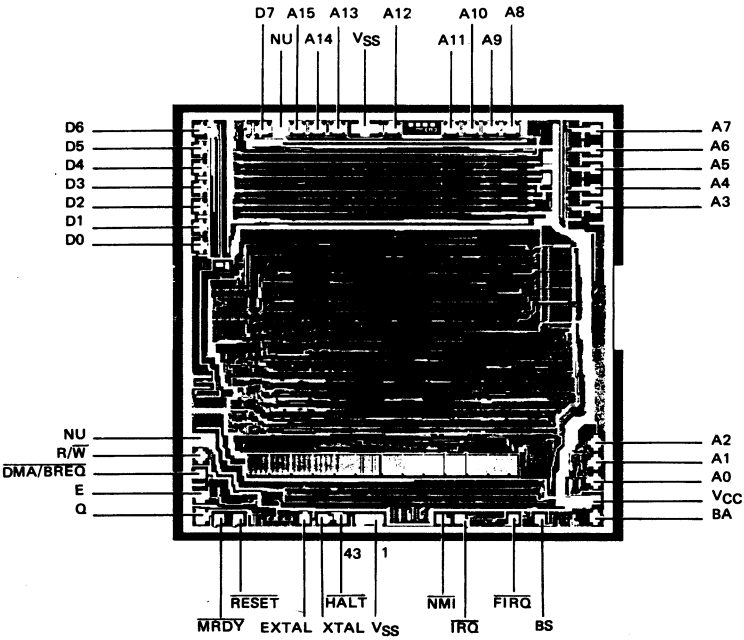
EF6800 COMPATIBLE

- Hardware – Interfaces with All 6800 Peripherals
- Software – Upward Source Code Compatible Instruction Set and Addressing Modes

HMOS

SPECIFICATIONS

PAD LAYOUT	: OAW.2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.08 x 5.06mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : V_{SS}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, EXTAL $\overline{RESET}$	V_{IH} V_{IHR}	V_{SS} + 2.0 V_{SS} + 4.0	– –	V_{CC} V_{CC}	V
Input Low Voltage	Logic, EXTAL, $\overline{RESET}$	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic	I_{in}	–	–	2.5	μA
dc Output High Voltage (I_{Load} = − 205 μA, V_{CC} = min) (I_{Load} = − 145 μA, V_{CC} = min) (I_{Load} = − 100 μA, V_{CC} = min)	D0-D7 A0-A15, R/$\overline{W}$, Q, E BA, BS	V_{OH}	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	– – –	– – –	V
dc Output Low Voltage (I_{Load} = 2.0 mA, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.5	V
Internal Power Dissipation *		P_{INT}	–	–	1.0	W
Capacitance * (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	D0-D7, $\overline{RESET}$ Logic Inputs, EXTAL, XTAL	C_{in}	– –	10 10	15 15	pF
	A0-A15, R/$\overline{W}$, BA, BS	C_{out}	–	–	15	pF
Frequency of Operation (Crystal or External Input)	EF6809	f_{XTAL}	0.4	–	4	MHz
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = max)	D0-D7 A0-A15, R/$\overline{W}$	I_{TSI}	– –	2.0 –	10 100	μA

* Not tested

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THOMSON COMPONENTS SEMICONDUCTEURS

J EF6809E

8-BIT MICROPROCESSOR UNIT (MPU)

The EF6809E is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the 6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The EF6809E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The EF6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems, or other MPUs.

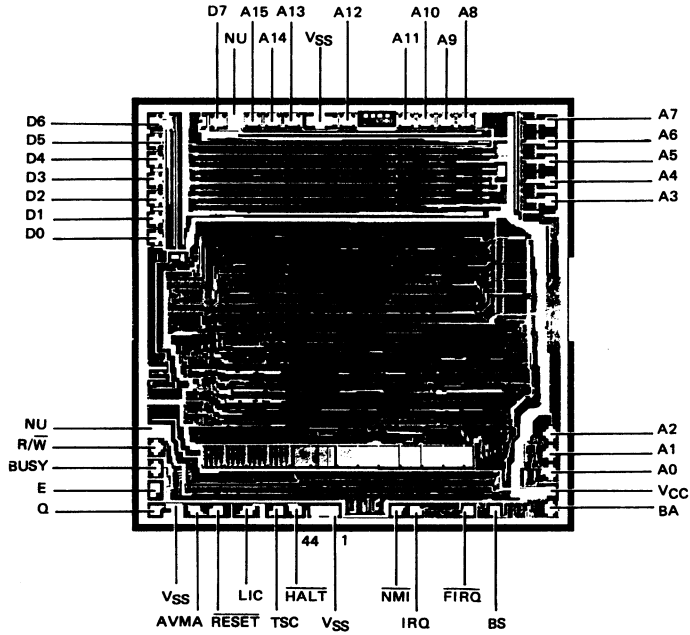
EF6800 COMPATIBLE

- Hardware – Interfaces with All 6800 Peripherals
- Software – Upward Source Code Compatible Instruction Set and Addressing Modes

HMOS

SPECIFICATIONS

PAD LAYOUT	: ODG.1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.02 x 5.04mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : V_{SS}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 ± 5%, V_{SS} = 0 Vdc, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, Q, $\overline{RESET}$	V_{IH}	V_{SS} + 2.0	–	–	V
	E	V_{IHR}	V_{SS} + 4.0	–	–	
		V_{IHC}	V_{CC} − 0.75	–	–	
Input Low Voltage	Logic, $\overline{RESET}$	V_{IL}	–	–	V_{SS} + 0.8	V
	E	V_{ILC}	–	–	V_{SS} + 0.4	V
	Q	V_{ILQ}	–	–	V_{SS} + 0.6	V
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic, Q, $\overline{RESET}$	I_{in}	–	–	2.5	μA
	E		–	–	100	
dc Output High Voltage		V_{OH}				V
(I_{Load} = −205 μA, V_{CC} = min)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = −145 μA, V_{CC} = min)	A0-A15, R/$\overline{W}$		V_{SS} + 2.4	–	–	
(I_{Load} = −100 μA, V_{CC} = min)	BA, BS, LIC, AVMA, BUSY		V_{SS} + 2.4	–	–	
dc Output Low Voltage (I_{Load} = 2.0 mA, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.5	V
Internal Power Dissipation (Measured at T_A = 0°C in Steady State Operation)		P_{INT}	–	–	1.0	W
Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	D0-D7, Logic Inputs, Q, $\overline{RESET}$	C_{in}	–	10	15	pF
	E		–	30	50	
	A0-A15, R/$\overline{W}$, BA, BS, LIC, AVMA, BUSY	C_{out}	–	10	15	pF
Frequency of Operation (E and Q Inputs)		f	0.1	–	1.5	MHz
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = max)	D0-D7	I_{TSI}	–	2.0	10	μA
	A0-A15, R/$\overline{W}$		–	–	100	

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THOMSON COMPONENTS SEMICONDUCTEURS

J EF6810

128 x 8-BIT STATIC RANDOM ACCESS MEMORY

The EF6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

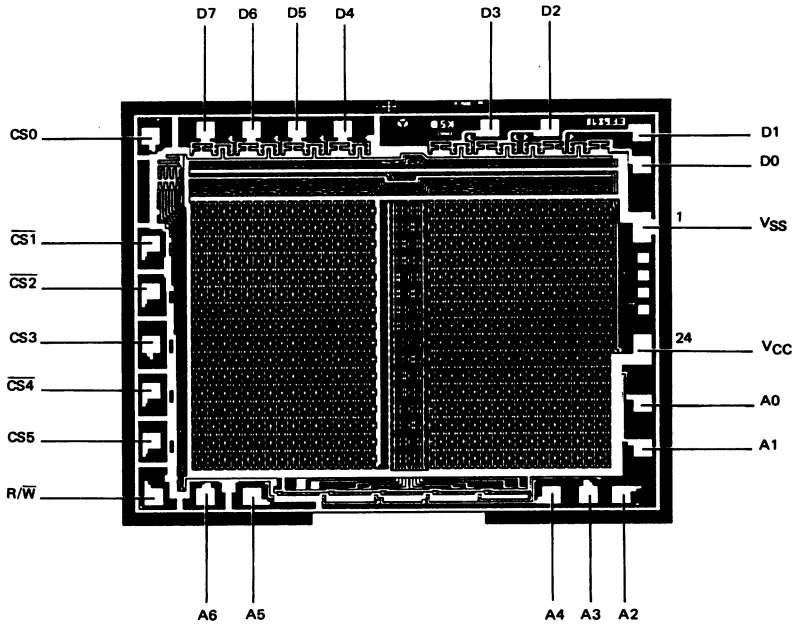
The memory is compatible with the 6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible

NMOS

SPECIFICATIONS

PAD LAYOUT	: OAA.2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.40 x 2.68mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-68) DIL24



Back side bias : V_{SS}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Current (A_n, R/$\overline{W}$, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	µA
Output High Voltage (I_{OH} = −205 µA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	V
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{TSI}	–	10	µA
Supply Current (V_{CC} = 5.25 V, All Other Pins Grounded) 1.0 MHz / 1.5, 2.0 MHz	I_{CC}	–	95	mA
Input Capacitance (A_n, R/$\overline{W}$, CS_n, $\overline{CS}_n$) (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	C_{in}	–	7.5	pF
Output Capacitance (D_n) (V_{out} = 0, T_{amb} = 25°C, f = 1.0 MHz, CSO = 0)	C_{out}	–	12.5	pF

READ CYCLE (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C)

Characteristic	Symbol	J EF6810 Min	J EF6810 Max	Unit
Read Cycle Time	$t_{cyc(R)}$	450	–	ns
Access Time	t_{acc}	–	450	ns
Address Setup Time *	t_{AS}	20	–	ns
Address Hold Time *	t_{AH}	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	ns
Read to Select Delay Time*	t_{RCS}	0	–	ns
Data Hold from Address *	t_{DHA}	10	–	ns
Output Hold Time*	t_H	10	–	ns
Data Hold from Read *	t_{DHR}	10	80	ns
Read Hold from Chip Select	t_{RH}	0	–	ns

WRITE CYCLE (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C)

Characteristic	Symbol	J EF6810 Min	J EF6810 Max	Unit
Write Cycle Time	$t_{cyc(W)}$	450	–	ns
Address Setup Time *	t_{AS}	20	–	ns
Address Hold Time *	t_{AH}	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	ns
Write to Chip Select Delay Time *	t_{WCS}	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	ns
Input Hold Time *	t_H	10	–	ns
Write Hold Time from Chip Select *	t_{WH}	0	–	ns

* Not tested

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.DSJEF6810

J EF6821

PERIPHERAL INTERFACE ADAPTER (PIA)

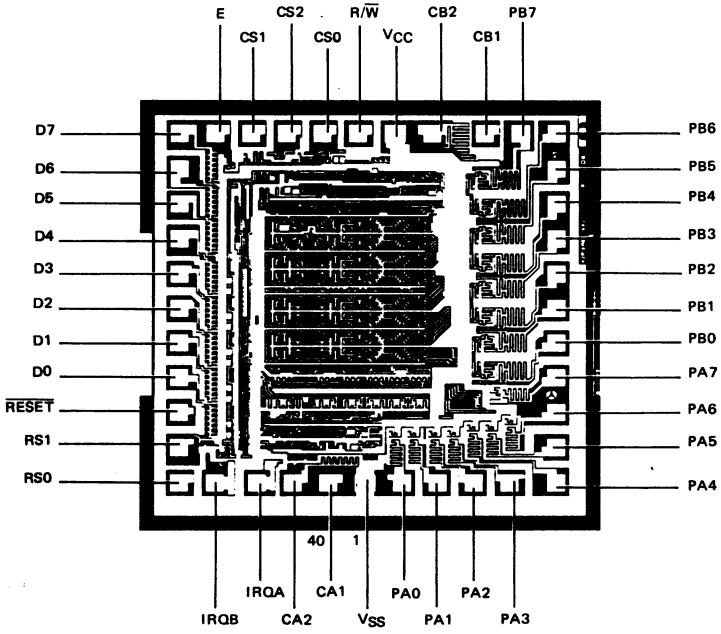
The EF6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the 6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

NMOS

SPECIFICATIONS

PAD LAYOUT	: OAG.2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 2.84 x 2.70mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-182) DIL40



Back side bias : V_{SS}

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MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, CS2)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	–	V
Input Low Voltage	V_{IL}	–	–	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V) *	I_{in}	–	1.0	2.5	µA
Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz) *	C_{in}	–	–	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Hi-Z Output Leakage Current	I_{OZ}	–	1.0	10	µA
Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz) *	C_{out}	–	–	5.0	pF
DATA BUS (D0-D7)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	–	V
Input Low Voltage	V_{IL}	–	–	V_{SS}+0.8	V
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	I_{IZ}	–	2.0	10	µA
Output High Voltage (I_{Load} = −205 µA)	V_{OH}	V_{SS}+2.4	–	–	V
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz) *	C_{in}	–	–	12.5	pF
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)					
Input Leakage Current (V_{in} = 0 to 5.25 V) R/$\overline{W}$, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	µA
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V) PB0-PB7, CB2	I_{IZ}	–	2.0	10	µA
Input High Current (V_{IH} = 2.4 V) PA0-PA7, CA2	I_{IH}	−200	−400	–	µA
Darlington Drive Current (V_O = 1.5 V) PB0-PB7, CB2	I_{OH}	−1.0	–	−10	mA
Input Low Current (V_{IL} = 0.4 V) PA0-PA7, CA2	I_{IL}	–	−1.3	−2.4	mA
Output High Voltage (I_{Load} = −200 µA) PA0-PA7, PB0-PB7, CA2, CB2	V_{OH}	V_{SS}+2.4	–	–	V
(I_{Load} = −10 µA) PA0-PA7, CA2		V_{CC}−1.0	–	–	
Output Low Voltage (I_{Load} = 3.2 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz) *	C_{in}	–	–	10	pF
POWER REQUIREMENTS					
Internal Power Dissipation (Measured at T_L = 0°C)	P_{INT}	–	–	550	mW

* Not tested

PERIPHERAL TIMING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C)

Characteristic	Symbol	J EF6821		Unit
		Min	Max	
Data Setup Time	t_{PDS}	200	–	ns
Data Hold Time	t_{PDH}	0	–	ns
Delay Time, Enable Negative Transition to CA2 Negative Transition	t_{CA2}	–	1.0	µs
Delay Time, Enable Negative Transition to CA2 Positive Transition	T_{RS1}	–	1.0	µs
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	µs
Delay Time from CA1 Active Transition to CA2 Positive Transition	t_{RS2}	–	2.0	µs
Delay Time, Enable Negative Transition to Data Valid	t_{PDW}	–	1.0	µs
Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2	t_{CMOS}	–	2.0	µs
Delay Time, Enable Positive Transition to CB2 Negative Transition	t_{CB2}	–	1.0	µs
Delay Time, Data Valid to CB2 Negative Transition	t_{DC}	20	–	ns
Delay Time, Enable Positive Transition to CB2 Positive Transition	t_{RS1}	–	1.0	µs
Control Output Pulse Width, CA2/CB2	PW_{CT}	500	–	ns
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	µ
Delay Time, CB1 Active Transition to CB2 Positive Transition	t_{RS2}	–	2.0	µs
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	t_{IR}	–	1.60	µs
Interrupt Response Time	t_{RS3}	–	1.0	µs
Interrupt Input Pulse Time	PW_I	500	–	ns
$\overline{RESET}$ Low Time	t_{RL}	1.0	–	µs

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6840

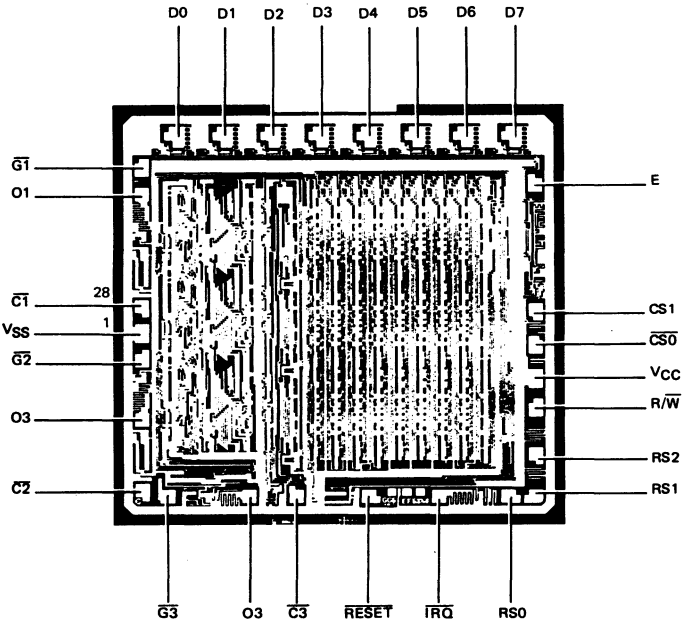
PROGRAMMABLE TIMER MODULE (PTM)

The EF6840 is a programmable subsystem component of the 6800 family designed to provide variable system time intervals.
The EF6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The EF6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

NMOS

SPECIFICATIONS

PAD LAYOUT	: ODL.2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.84 x 4.02mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-132) DIL28



Back side bias : V_{SS}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range − T_L to T_H	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)		I_{in}	–	1.0	2.5	µA
Hi-Z (Off State) Input Current (V_{in} = 0.5 to 2.4 V)	D0-D7	I_{TSI}	–	2.0	10	µA
Output High Voltage (I_{Load} = −205 µA) (I_{Load} = −200 µA)	 D0-D7 Other Outputs	V_{OH}	 V_{SS} + 2.4 V_{SS} + 2.4	 – –	 – –	V
Output Low Voltage (I_{Load} = 1.6 mA) (I_{Load} = 3.2 mA)	 $\overline{IRQ}$, D0-D7 O1-O3	V_{OL}	 – –	 – –	 V_{SS} + 0.4 V_{SS} + 0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	µA
Internal Power Dissipation (Measured at = T_L)		P_{INT}	–	470	700	mW
Input Capacitance * (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	 D0-D7 All Others	C_{in}	 – –	 – –	 12.5 7.5	pF
Output Capacitance * (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	 $\overline{IRQ}$ O1, O2, O3	C_{out}	 – –	 – –	 5.0 10	pF

* Not tested

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Ref.DSJEF6840

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6850

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The EF6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the EF6800 Microprocessing Unit.

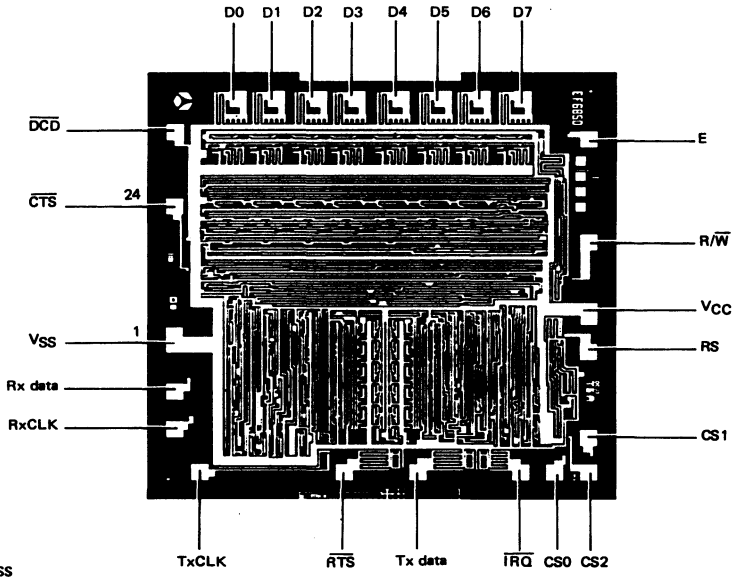
The bus interface of the EF6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided.

- 8- and 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷ 1, ÷ 16, and ÷ 64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One- or Two-Stop Bit Operation

NMOS

SPECIFICATIONS

PAD LAYOUT	: OCJ.2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.06 x 2.86mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-68) DIL24



Back side bias : V_{SS}

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MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	–	V
Input Low Voltage		V_{IL}	–	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/$\overline{W}$, CS0, CS1, $\overline{CS2}$, Enable RS, Rx D, Rx C, $\overline{CTS}$, $\overline{DCD}$	I_{in}	–	1.0	2.5	µA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0-D7	I_{TSI}	–	2.0	10	µA
Output High Voltage (I_{Load} = −205 µA, Enable Pulse Width < 25 µs)	D0-D7	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = −100 µA, Enable Pulse Width < 25 µs)	Tx Data, $\overline{RTS}$		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mA, Enable Pulse Width < 25 µs)		V_{OL}	–	–	V_{SS} + 0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	µA
Internal Power Dissipation (Measured at T_{amb} = 0°C)		P_{INT}	–	300	525*	mW
Internal Input Capacitance ** (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	D0-D7	C_{in}	–	10	12.5	pF
	E, Tx CLK, Rx CLK, R/$\overline{W}$, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$		–	7.0	7.5	
Output Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	RTS, Tx Data	C_{out}	–	–	10	pF
	$\overline{IRQ}$		–	–	5.0	

*For temperatures less than T_{amb} = 0°C, P_{INT} maximum will increase.

** Not tested

SERIAL DATA TIMING CHARACTERISTICS

Characteristic		Symbol	J EF6850 Min	J EF6850 Max	Unit
Data Clock Pulse Width, Low	÷16, ÷64 Modes	PW_{CL}	600	–	ns
	÷1 Mode		900	–	
Data Clock Pulse Width, High	÷16, ÷64 Modes	PW_{CH}	600	–	ns
	÷1 Mode		900	–	
Data Clock Frequency	÷16, ÷64 Modes	f_C	–	0.8	MHz
	÷1 Mode		–	500	kHz
Data Clock-to-Data Delay for Transmitter		t_{TDD}	–	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDS}	250	–	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	250	–	ns
Interrupt Request Release Time		t_{IR}	–	1.2	µs
Request-to-Send Delay Time		t_{RTS}	–	560	ns
Input Rise and Fall Times (or 10% of the pulse width if smaller)		t_r, t_f	–	1.0	µs

These specifications are subjet to change without notice.
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Ref.DSJEF6850

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6852

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

The EF6852 Synchronous Serial Data Adapter provides a bidirectional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the 6800 Microprocessor systems.

The bus interface of the EF6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

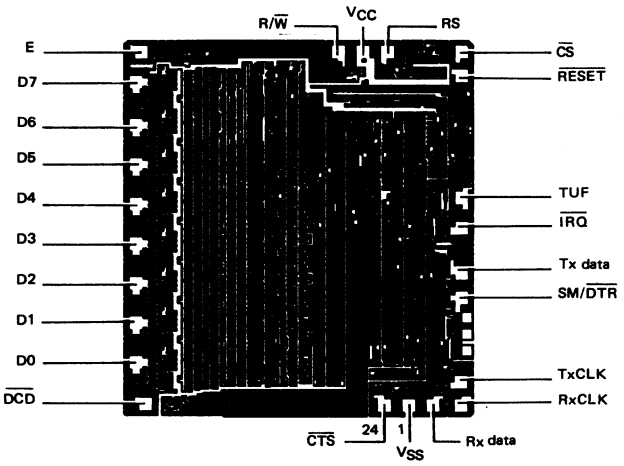
Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One- or Two-Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 1.5 MHz Transmission
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- 7-, 8-, or 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status

NMOS

SPECIFICATIONS

PAD LAYOUT	: DAB.1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.50 x 3.86mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-68) DIL24



Back side bias : V_{SS}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	–	V
Input Low Voltage		V_{IL}	–	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	Tx CLK, Rx CLK, Rx Data, Enable, $\overline{RESET}$, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$	I_{in}	–	1.0	2.5	µA
Hi-Z (Off-State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V)	D0-D7	I_{IZ}	–	2.0	10	µA
Output High Voltage (I_{Load} = −205 µA, Enable Pulse Width < 25 µs)	D0-D7	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = −100 µA, Enable Pulse Width < 25 µs)	TX Data, $\overline{DTR}$, TUF		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mA, Enable Pulse Width < 25 µs)		V_{OL}	–	–	V_{SS} + 0.4	V
Output Leakage Current (Off-State) (V_{OH} = 2.4 V)	$\overline{IRQ}$	I_{OZ}	–	1.0	10	µA
Internal Power Dissipation (Measured at T_{amb} = 0°C)*		P_{INT}	–	300	525*	mW
Input Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	D0-D7	C_{in}	–	–	12.5	pF
	All Other Inputs		–	–	7.5	
Output Capacitance (V_{in} = 0, T_{amb} = 25°C, f = 1.0 MHz)	Tx Data, SM/$\overline{DTR}$, TUF	C_{out}	–	–	10	pF
	$\overline{IRQ}$				5.0	

*For temperatures below 0°C, the maximum value of P_{INT} will increase.

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	J EF6852		Unit
		Min	Max	
Serial Clock Pulse Width, Low	PW_{CL}	700	–	ns
Serial Clock Pulse Width, High	PW_{CH}	700	–	ns
Serial Clock Frequency (Rx CLK, Tx CLK)	f_C	–	600	kHz
Receive Data Setup Time	t_{RDSU}	350	–	ns
Receive Data Hold Time	t_{RDH}	350	–	ns
Sync Match Delay Time	t_{SM}	–	1.0	µs
Clock-to-Data Delay for Transmitter	T_{DD}	–	1.0	µs
Transmitter Underflow	t_{TUF}	–	1.0	µs
$\overline{DTR}$ Delay Time	t_{DTR}	–	1.0	µs
Interrupt Request Release Time	t_{IR}	–	1.6	µs
$\overline{RESET}$ Pulse Width	t_{RESET}	1.0	–	µs
$\overline{CTS}$ Setup Time	t_{CTS}	200	–	ns
$\overline{DCD}$ Setup Time	t_{DCD}	500	–	ns
Input Rise and Fall Times (Except Enable)	t_r, t_f	–	1.0*	µs

*1.0 µs or 10% of the pulse width, whichever is smaller

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.DSJEF6852

THOMSON COMPONENTS SEMICONDUCTEURS

J EF6854

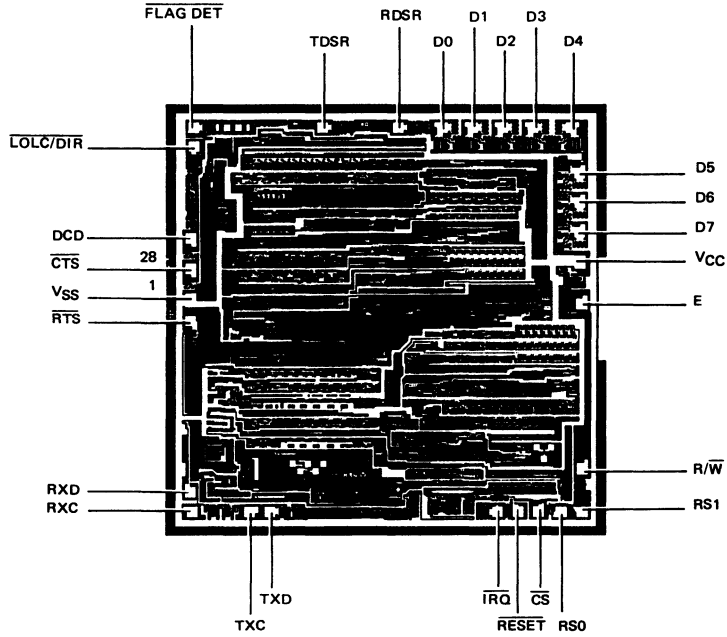
ADVANCED DATA-LINK CONTROLLER (ADLC)

The EF6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High-Level Data-Link Control (HDLC) and Synchronous Data-Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

NMOS

SPECIFICATIONS

PAD LAYOUT	: OFP.1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 4.40 x 4.42mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-132) DIL28



Back side bias : V_{SS}

April 1987-1/2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{amb}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	–	V
Input Low Voltage		V_{IL}	–	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	All Inputs Except D0-D7	I_{in}	–	1.0	2.5	µA
Hi-Z (Off-State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V)	D0-D7	I_{IZ}	–	2.0	10	µA
dc Output High Voltage (I_{Load} = − 205 µA)	D0-D7	V_{OH}	V_{SS} + 2.4	–	–	V
(V_{Load} = − 100 µA)	All Others		V_{SS} + 2.4	–	–	
dc Output Low Voltage (I_{Load} = 1.6 mA))		V_{OL}	–	–	V_{SS} + 0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	$\overline{IRQ}$	I_{OZ}	–	1.0	10	µA
Internal Power Dissipation (measured at T_{amb} = 0°C)		P_{INT}	–	–	850*	mW
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7	C_{in}	–	–	12.5	pF
	All Other Inputs		–	–	7.5	
	$\overline{IRQ}$	C_{out}	–	–	5.0	pF
	All Others		–	–	10	

* For temperatures below 0°C, P_{INT} will increase.

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

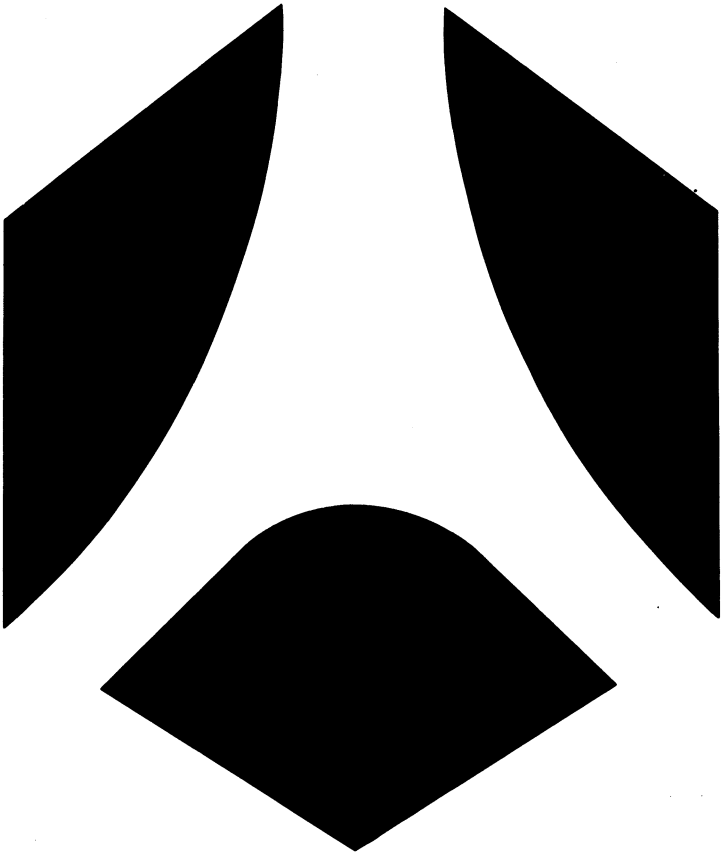
Characteristic	Symbol	J EF6854		Unit
		Min	Max	
Clock Pulse Width, Low (RxC, TxC)	PW_{CL}	700	–	ns
Clock Pulse Width, High (RxC, TxC)	PW_{CH}	700	–	ns
Serial Clock Frequency (RxC, TxC)	f_{SC}	–	0.66	MHz
Receive Data Setup Time	t_{RDSU}	150	–	ns
Receive Data Hold Time	t_{RDH}	60	–	ns
Request-to-Send Delay Time	t_{RTS}	–	680	ns
Clock-to-Data Delay for Transmitter	t_{TDD}	–	300	ns
Flag Detect Delay Time	t_{FD}	–	680	ns
$\overline{DTR}$ Delay Time	t_{DTR}	–	680	ns
Loop On-Line Control Delay Time	t_{LOC}	–	680	ns
RDSR Delay Time	t_{RDSR}	–	540	ns
TDSR Delay Time	t_{TDSR}	–	540	ns
Interrupt Request Release Time	t_{IR}	–	1.2	µs
$\overline{RESET}$ Pulse Width	t_{RESET}	1.0	–	µs
Input Rise and Fall Times (Except Enable) (0.8 V to 2.0 V)	t_r, t_f	–	1.0*	µs

*1.0 µs or 10% of the pulse width, whichever is smaller.

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

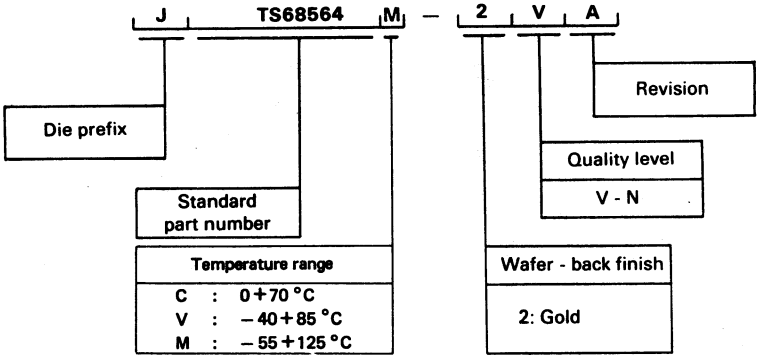
Printed in France

Ref.DSJEF6854



68000 microprocessors & peripherals

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J TS68000		X	X					X	A
J TS68008		X	X					X	A
J TS68230		X	X					X	A
J TS68483		X	X					X	A
J TS68564		X	X					X	A
J TS68901		X	X					X	A
J TS68HC901		X	X					X	A
J TS68931		X	X					X	A

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68000

16-/32-BIT MICROPROCESSOR

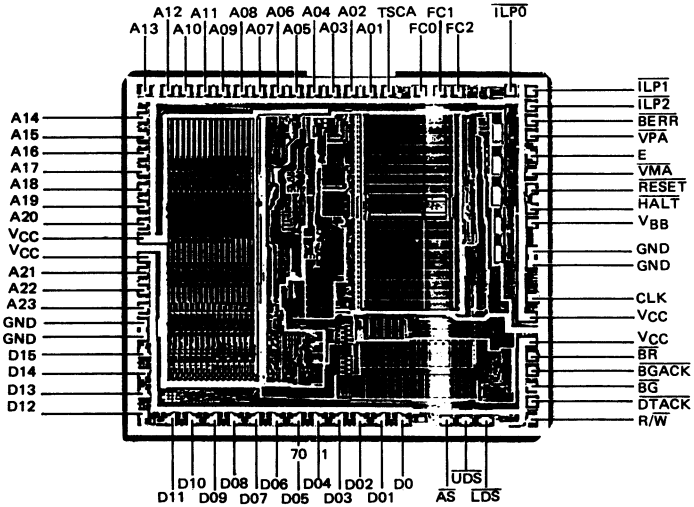
The TS68000 is the first implementation of the 68000 16/32 microprocessor architecture. The TS68000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data buses. It is completely code-compatible with the TS68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the TS68020 32-bit implementation of the architecture. Any user-mode programs written using the TS68000 instruction set will run unchanged on the TS68008 and TS68020. This is possible because the user programming model is identical for all three processors and the instruction sets are proper sub-sets of the complete architecture.
The resources available to the TS68000 user consist of the following :

- 16 32-bit data and address registers
- 16 megabyte direct addressing range
- 56 powerful instruction types
- Operations on five main data types
- Memory mappel I/O
- 14 addressing modes
- 2 available versions : 8 MHz (H 1), 12.5 MHz (H2)

HMOS
HMOS2

SPECIFICATIONS

PAD LAYOUT	: H1 OEL1 : H2 OKC1
PAD SIZE	: H1 0.1 x 0.1mm : H2 0.08 x 0.08mm
DIE SIZE	: H1 7.38 x 6.52mm : H2 6.015 x 5.04mm : ± 0.05
DIE THICKNESS	: H1 0.375mm : H2 0.375mm ± 0.025
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	: (CB-365 DIL64
LOT CASE	



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	0.3 to + 7.0	V
Input Voltage	V_{IN}	0.3 to + 7.0	V
Operating Temperature Range	T_{oper}	– 55 to + 125	°C
Storage Temperature	T_{stg}	55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 5.0 V ± 5% ; GND = 0 V ; T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	2.0	–	V_{CC}	V
Input low voltage	V_{IL}	GND–0.3	–	0.8	V
Input leakage Current @ 5.25 V $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACR}$ CLK, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{VPA}$ $\overline{HALT}$, $\overline{RESET}$	I_{IN}	– – –	– – –	– 2.5 20	– µA
Three-State (Off State Input Current @ 2.4 V/0.4 $\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	–	–	20	µA
Output High Voltage (I_{OH} = – 400 µA) E* E, $\overline{AS}$, A1-A23, $\overline{BG}$, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	V_{CC}–0.75 – 2.4	– – –	– – –	 V –
Output low voltage (I_{OL} = 1.6 mA) $\overline{HALT}$ (I_{OL} = 3.2 mA) A1-A23, BG, FC0-FC2 (I_{OL} = 5.0 mA) $\overline{RESET}$ (I_{OL} = 5.3 mA) E, AS, D0-D15, $\overline{LDS}$, R/$\overline{W}$ $\overline{UDS}$, $\overline{VMA}$	V_{OL}	– – – – –	– – – – –	0:5 0.5 0.5 0.5 –	 – V – –
Power supply current	I_{CC}	–	–	290	mA
Capacitance (V_I = 0 V, T_{amb} = 25°C ; Frequency = 1 MHz)**	C_I	–	–	20.0	pF

* With external pullup resistor of 1.1 kΩ

** Capacitance is periodically sampled rather than 100 % tested.

CLOCK TIMING

Characteristic	Symbol	H1			H2			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency of Operation	f	4.0	–	8.0	4.0	–	12.6	MHz
Cycle time	t_{cyc}	125	–	250	80	–	250	ns
Clock Pulse Width	t_{CL} t_{CH}	55 55	– –	125 125	35 35	– –	125 125	ns
Rise and Fall Times	t_{Cr} t_{Cf}	– –	– –	10 10	– –	– –	5 5	ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/JTS68000

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68008

8-/32-BIT MICROPROCESSOR WITH 8-BIT DATA BUS

The TS68008 is a member of the TS68000 family of advanced microprocessors. This device allows the design of cost effective systems using 8-bit data buses while providing the benefits of a 32-bit microprocessor architecture. The performance of the TS68008 is greater than any 8-bit microprocessor and superior to several 16-bit microprocessors.

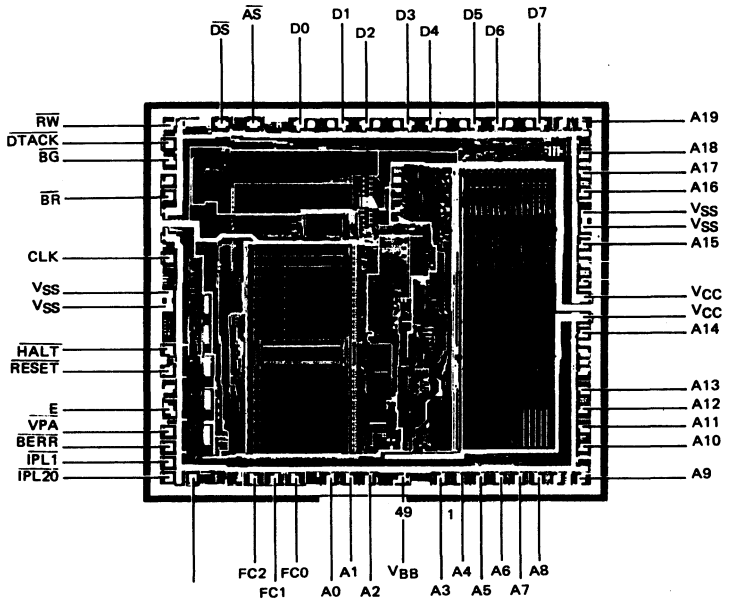
- 1732-bit Data and Address Registers.
- 56 Basic Instruction Types.
- Extensive Exception Processing.
- Memory Mapped I/O.
- 14 Addressing Modes.
- 1 Mbyte Linear Addressing Space.
- Complete Code Compatibility with the TS68000

A system implementation based on an 8-bit data bus reduces system cost in comparison to 16-bit systems due to a more effective use of components and the fact that byte-wide memories and peripherals can be used much more effectively. In addition, the non-multiplexed address and data buses eliminate the need for external demultiplexers, thus further simplifying the system.

HMOS

SPECIFICATIONS

PAD LAYOUT	: OFD2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 6.68 x 5.88mm
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	0.3 to + 7.0	V
Input Voltage	V_{IN}	0.3 to + 7.0	V
Operating Temperature Range	T_{oper}	− 40 to + 85	°C
Storage Temperature	T_{stg}	55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 5.0 V ± 5% ; GND = 0 V ; T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Input high voltage	V_{IH}	2.0	–	V_{CC}	V
Input low voltage	V_{IL}	GND–0.3	–	0.8	V
Input leakage current @5.25 V $\overline{BERR}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0/2}$, $\overline{IPL1}$, $\overline{VPA}$, $\overline{HALT}$, $\overline{RESET}$, $\overline{BGACK}$	I_{IN}	–	–	20	µA
Hi-Z (Off State) input current @2.4 V/0.4 V A0-A19, $\overline{AS}$, D0-D7, FC0-FC2, $\overline{DS}$, R/$\overline{W}$	I_{TSI}	–	–	20	µA
Output high voltage (I_{OH} = − 400 µA) E, A0-A19, AS, BG, D0-D7, FC0-FC2, $\overline{DS}$, R/$\overline{W}$, $\overline{VMA}$	V_{OH}	– 2.4	– –	– –	V –
Output low voltage (I_{OL} = 1.6 mA) $\overline{HALT}$ (I_{OL} = 3.2 mA) A0-A-19, $\overline{BG}$, FC0-FC2 (I_{OL} = 5.0 mA) $\overline{RESET}$ (I_{OL} = 5.3 mA) E, $\overline{AS}$, D0-D7, $\overline{DS}$, R/$\overline{W}$	V_{OL}	– – – –	– – – –	0.5 0.5 0,5 0,5	– V
Power Dissipation, * T_{amb} = 0°C	P_D	–	–	1.5	W
Capacitance (V_I = 0 V, T_{amb} = 25°C, Frequency = 1 MHz)**	C_I	–	–	20.0	pF

* During normal operation instantaneous V_{CC} current requirements may be as high as 1.5 A
** Capacitance is periodically sampled rather than 100 % tested.

CLOCK TIMING

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Frequency of operation	f	2.0	–	8.0	MHz
Cycle time	t_{cyc}	125	–	500	ns
Clock pulse width	t_{CL} t_{CH}	55 55	– –	250 250	ns
Rise and fall times	t_{Cr} t_{Cf}	– –	– –	10 10	ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJTS68008

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68230

PARALLEL INTERFACE/TIMER

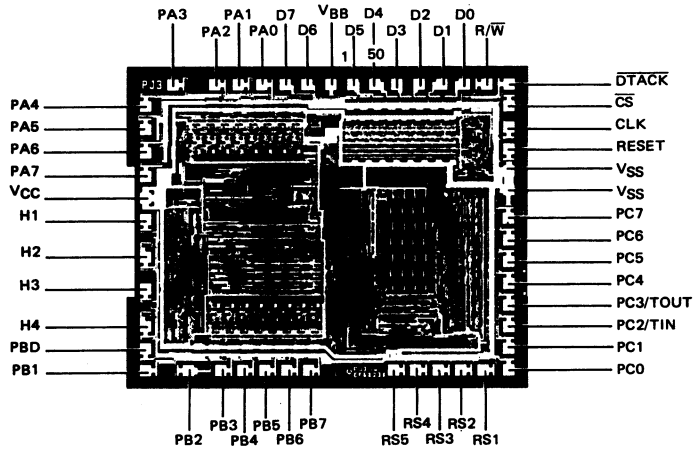
The TS68230 parallel interface/timer (PI/T) provides versatile double buffered parallel interfaces and a system oriented timer for TS68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is an input or output. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or auto-vectored interrupts, and also provide a DMA request pin for connection to the 68440 direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.

- TS68000 Bus Compatible
- Port Modes Include :
  Bit I/O
  Unidirectional 8 Bit and 16 Bit
  Bidirectional 8 Bit and 16 Bit
- Programmable Handshaking Options
- 24-Bit Programmable Timer Modes
- Five Separate Interrupt Vectors
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility.

HMOS

SPECIFICATIONS

PAD LAYOUT	: OFH2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 4.00 x 3.34mm
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	0.3 to + 7.0	V
Input Voltage	V_{IN}	0.3 to + 7.0	V
Operating Temperature Range	T_{oper}	− 55 to + 125	°C
Storage Temperature	T_{stg}	55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 5.0 V ± 5% ; GND = 0 V ; T_{amb} = 25°C (unless otherwise specified)

Characteristics		Symbol	Min.	Typ.	Max.	Unit.
Input high voltage	All inputs	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input low voltage	All inputs	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input leakage current (V_{IN} = 0 to 5.25 V) H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$		I_{IN}	–	–	10.0	µA
Hi-Z (Off State) input current (V_{in} = 0.4 to 2.4) $\overline{DTACK}$, PC0-PC7, D0-D7 H2, H4, PA0-PA7, PB0-PB7		I_{TSI}	– − 0.1	– –	20 − 1.0	µA mA
Output high voltage (I_{Load} = − 400 µA, V_{CC} = min) (I_{Load} = − 150 µA, V_{CC} = min) (I_{Load} = − 100 µA, V_{CC} = min)	$\overline{DTACK}$, D0-D7 H2, H4, PB0-PB7, PA0-PA7 PC0-PC7	V_{OH}	V_{SS} + 2.4	–	–	V
Output low voltage (I_{Load} = 8.8 mA, V_{CC} = min) (I_{Load} = 5.3 mA, V_{CC} = min) (I_{Load} = 2.4 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$ D0-D7, $\overline{DTACK}$ PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	–	–	0.5	V
Internal power dissipation (measured at T_{amb} = 0°C)		P_{INT}	–	–	750	mW
Input Capacitance (V_I = 0, T_{amb} = 25°C, f = 1 MHz)		C_I	–	–	15	pF

CLOCK TIMING

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Frequency of operation	f	2.0	–	8.0	MHz
Cycle time	t_{cyc}	125	–	500	ns
Clock pulse width	t_{CL} t_{CH}	55 55	– –	250 250	ns
Rise and fall times	t_{Cr} t_{Cf}	– –	– –	10 10	ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJTS68230

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68483

ADVANCED GRAPHIC AND ALPHANUMERIC CONTROLLER

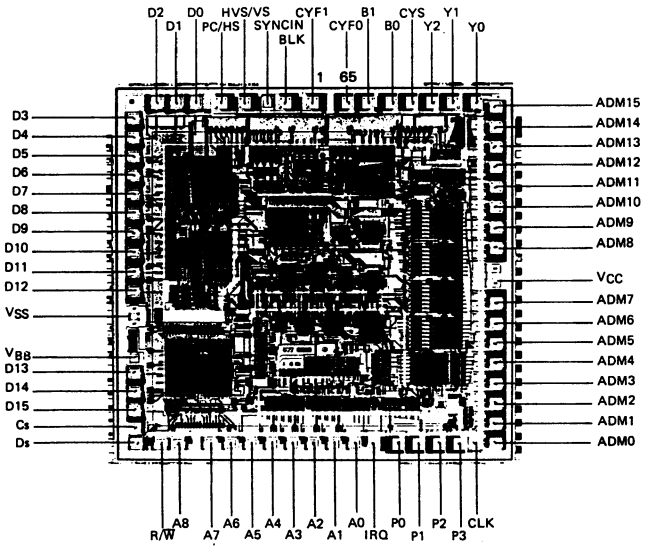
The TS68483 is an advanced color graphic processor that drastically reduces the CPU software overhead for all graphic tasks in medium and high range graphic applications such as business and personal computer, industrial monitoring system and CAD systems.

- Fully programmable timing generator.
- Alphanumeric and graphic drawing capability.
- Easy to use and powerful command set:
  - VECTOR, ARC, CIRCLE with dot or pen concept and programmable line style,
  - Flexible area fill command with tiling pattern,
  - Very fast block move operation,
  - Character drawing command, any size and fonts available.
- Large frame buffer addressing space (8 megabyte) up to 16 planes of 2048 x 2048.
- Up to 256 color capabilities.
- Mask bit planes for general clipping purpose.
- Frame buffer can be built with standard 64K or 256K DRAM or Dual-Port-Memories (Video-RAM).
- External Synchronization capability.
- On chip video shift registers for Dot rate less than 15 Megadots/s.
- 8 or 16-bit bus interface compatible with market standard microprocessors.
- HMOS 2 technology.

HMOS2

SPECIFICATIONS

PAD LAYOUT	: OEK3
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 6.00 x 5.64mm
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-523) MO-047-AE



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	− 0.3 to 7.0	V
Input voltage	V_{IN}*	− 0.3 to 7.0	V
Operating temperature range	T_{oper}	− 55 to + 125	°C
Storage temperature range	T_{stg}	− 55 to + 150	°C
Max power dissipation	P_{Dm}	1.5	W

* With respect to V_{SS}

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristics	Symbol	Min.	Typ.	Max.	Unit.
Supply voltage	V_{CC}	4.75	5	5.25	V
Input low voltage	V_{IL}	− 0.3	–	0.8	V
Input high voltage clock other inputs	V_{IH}	2.5 2	– –	– V_{CC}	V
Input leakage current	I_{IN}	–	–	10	µA
Output high voltage (I_{load} = − 500 µA)	V_{OH}	2.4	–	–	V
Output low voltage I_{load} = 4 mA ; ADM (0:15) I_{load} = 1 mA ; other outputs	V_{OL}	–	–	0.4	V
Power dissipation	P_D	–	800	–	mW
Input capacitance	C_I	–	–	15	pF
Three state (off state) input current	I_{TSI}	–	–	10	µA

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJTS68483

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68564

SERIAL INPUT/OUTPUT CONTROLLER

The TS68564 SIO is a dual-channel, Serial Input/Output Controller, designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller ; however, within that role, it is systems software configurable so that it may be optimized for any given serial data communications application.

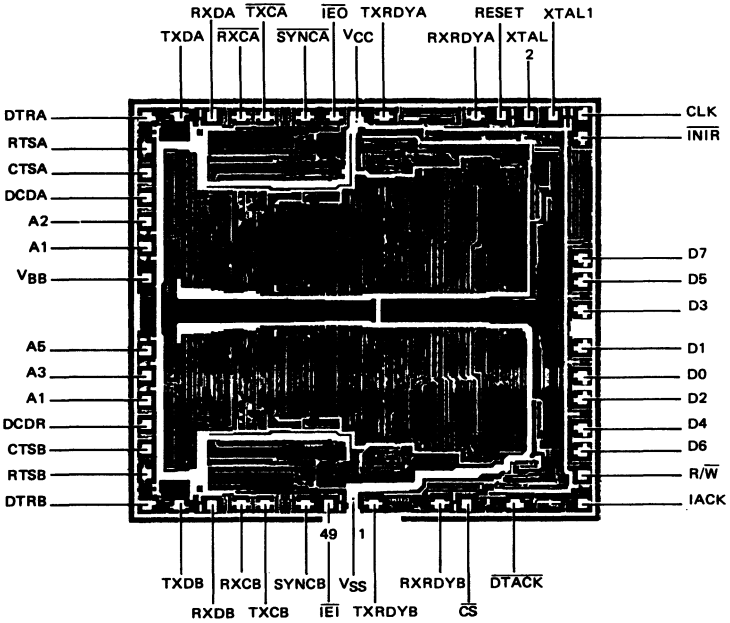
The TS68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The TS68564 can generate and check CRC codes in any synchronous mode and may be programmed to check data integrity in various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

HMOS

SPECIFICATIONS

PAD LAYOUT	: OIU1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 6.25 x 6.75mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{IN}	− 0.3 to + 7.0	V
Operating temperature range	Toper	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Temperature under bias		− 25 to + 100	°C
Power dissipation	P_D	1.5	W

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Input high voltage (all inputs)	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input low voltage (all inputs)	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Power supply current (outputs open)	I_{LL}	–	–	190	mA
Input leakage current (V_{IN} = 0 to 5.25)	I_I	–	–	± 10	µA
Three-state (off state) input current ($0 < V_{in} < V_{CC}$) $\overline{DTACK}$, D0-D7, SYNC, $\overline{TxC}$, $\overline{RxC}$, $\overline{INTR}$	I_{TSI}	... – –	– – –	– 20 ± 10	µA
Output high voltage (I_{LOAD} = − 400 µA, V_{CC} = min) $\overline{DTACK}$, D0-D7 (I_{LOAD} = − 150 µA, V_{CC} = min) All other outputs (except XTAL2 & $\overline{INTR}$)*	V_{OH}	V_{SS} + 2.4	–	–	V
Output low voltage (I_{LOAD} = 5.3 mA, V_{CC} = min) $\overline{INTR}$, $\overline{DTACK}$, D0-D7 (I_{LOAD} = 2.4 mA, V_{CC}= min) All other outputs (except XTAL2)*	V_{OL}	–	–	0.05	V

XTAL2 special $\overline{INTR}$ (open drain)

CAPACITANCE T_{amb} = 25°C, F = 1 MHz

Characteristic		Symbol	Min.	Typ.	Max.	Unit.
Input Capacitance	$\overline{CS}$, $\overline{IACK}$ All others	C_I	– –	– –	15 10	pF
Tri-state Output capacitance		C_{out}	–	–	10	pF

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.:DS/TS68564

J TS68901

MULTI-FUNCTION PERIPHERAL

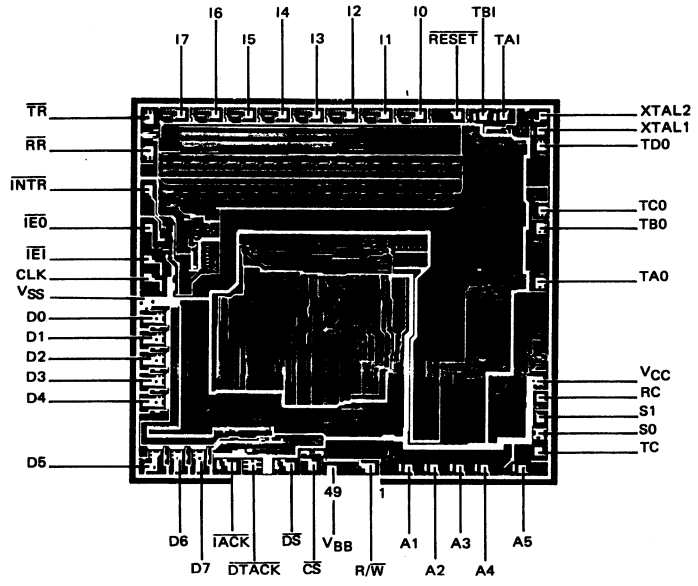
The TS68901 MFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are:

- Eight parallel I/O lines
- Interrupt controller for 16 sources
- Four timers
- Single channel full duplex USART

HMOS

SPECIFICATIONS

PAD LAYOUT	: OIT1
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.94 x 5.50mm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



Back side bias : V_{BB}

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{IN}	− 0.3 to + 7.0	V
Operating temperature range	Toper	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Power dissipation	P_D	30	W

ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Input high voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3	–	0.8	V
Output high voltage, except $\overline{DTACK}$ (I_{OH} = − 120 µA)	V_{OH}	2.4	–	–	V
Output low voltage, except $\overline{DTACK}$ (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.5	V
Power supply current (outputs open)	I_{LL}	–	–	180	mA
Input leakage current (V_{IN} = 0 to V_{CC})	I_{LI}	–	–	± 10	µA
Hi-Z output leakage current in float (V_{out} = 2.4 to V_{CC})	I_{LOH}	–	–	10	µA
Hi-Z output leakage current in float (V_{out} = 0.5 V)	I_{LOH}	–	–	− 10	µA
$\overline{DTACK}$ output source current (V_{out} = 2.4 V)	I_{OH}	–	–	− 400	µA
$\overline{DTACK}$ output sink current (V_{out} = 0.5 V)	I_{OL}	–	–	5.3	mA

CAPACITANCE T_{amb} = 25°C, F = 1 MHz

Characteristic		Symbol	Min.	Typ.	Max.	Unit.
Input Capacitance	$\overline{CS}$, $\overline{IACK}$	C_{IN}	–	–	10	pF
	All others		–	–	10	
Hi-Z Output capacitance		C_{Out}	–	–	10	pF

CLOCK TIMING

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Frequency of operation	f	1.0	–	4.0	MHz
Cycle time .	t_{cyc}	250	–	1000	ns
Clock pulse width	t_{CL}	110	–	250	ns
	t_{CH}	110	–	250	
Rise and fall times	t_{Cr}	–	–	15	ns
	t_{Cf}	–	–	15	

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/JTS68901

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68HC901

MULTI-FUNCTION PERIPHERAL

The TS68HC901 muli-function peripheral (CMFP) is a member of the 68000 Family of peripherals and the CMOS version of the MK68901. The CMFP directly interfaces to the 68000 processor via an asynchronous bus structure and can also support both multiplexed and non multiplexed buses. Both vectored, non vectored and polled interrupt schemes are supported, with the CMFP providing unique vector number generation for each of its 16 interrupt sources. Additionally, handshake lines are provided to facilitate DMAC interfacing.

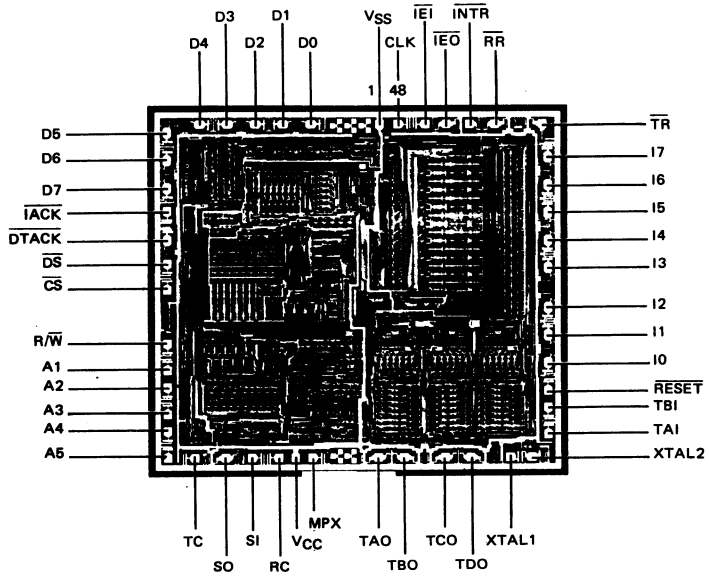
The TS68HC901 performs many of the functions common to most microprocessor-based systems. The resources available to the user include :

- Eight Individually Programmable I/O Pins with Interrupt Capability
- 16-Source Interrupt Controller with Individual Source Enabling and Masking
- Four Timers, Two of which are Multi-Mode Timers
- Timers may be used as Baud Rate Generators for the Serial Channel
- Single-Channel Full-Duplex Universal Synchronous/Asynchronous Receiver-Transmitter (USART) that Supports Asynchronous and with the Addition of a Polynominal Generator Checker Supports Byte Synchronous Formats.

HCMOS

SPECIFICATIONS

PAD LAYOUT	: OIS2A
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 5.82 x 5.26mmm ± 0.05
DIE THICKNESS	: 0.375mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



Back side bias : Isolated

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{IN}	− 0.3 to + 7.0	V
Operating temperature range	Toper	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Power dissipation	P_D	30	W

ELECTRICAL OPERATING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Input high voltage except XTAL1, XTAL2	V_{IH}	2.0	–	–	V
Input high voltage XTAL1, XTAL2	V_{IH}	V_{DD} − 1.5	–	V_{DD} + 0.3	V
Input low voltage	V_{IL}	− 0.3	–	0.8	V
Output high voltage, except $\overline{DTACK}$ (I_{OH} = − 120 µA)	V_{OH}	4.1	–	–	V
Output low voltage, except $\overline{DTACK}$ (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.5	V
Power supply current (outputs open)	I_{LL}	–	–	8	mA
Input leakage current (V_{in} = 0 to V_{CC})	I_{LI}	–	–	± 10	µA
Hi-Z output leakage current in float (V_{out} = 2.4 to V_{CC})	I_{LOH}	–	–	10	µA
Hi-Z output leakage current in float (V_{out} = 0.5 V)	I_{LOL}	–	–	− 10	µA
$\overline{DTACK}$ output source current (V_{out} = 2.4 V)	I_{OH}	–	–	− 400	µA
$\overline{DTACK}$ output sink current (V_{out} = 0.5 V)	I_{OL}	–	–	5.3	mA
Pull down resistor	R_{MPX}	0.5	–	4	MΩ

CAPACITANCE T_{amb} = 25°C, F = 1 MHz

Characteristic		Symbol	Min.	Typ.	Max.	Unit.
Input Capacitance	$\overline{CS}$, $\overline{IACK}$ All others	C_{IN}	– –	– –	10 10	pF
Hi-Z Output capacitance		C_{Out}	–	–	10	pF

CLOCK TIMING

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Frequency of operation	f	1.0	–	4.0	MHz
Cycle time .	t_{cyc}	250	–	1000	ns
Clock pulse width	t_{CL} t_{CH}	110 110	– –	250 250	ns
Rise and fall times	t_{Cr} t_{Cf}	– –	– –	15 15	ns

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS/JTS68HC901

THOMSON COMPONENTS SEMICONDUCTEURS

J TS68931

PROGRAMMABLE SIGNAL PROCESSOR

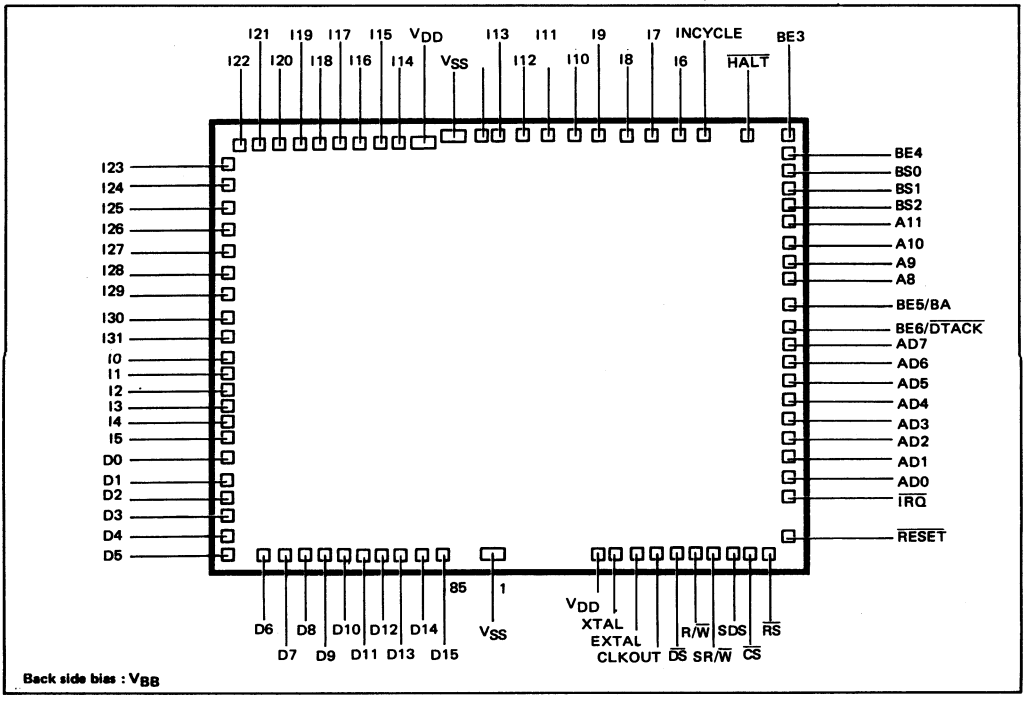
The TS68931 (Programmable Signal Processor) is a high-speed general purpose signal and arithmetic processor with on-chip memory, multiplier, ALU, accumulators and I/Os. It is organised in a parallel/pipeline structure to execute simultaneously one ALU, function, multiplication, two reads and one write operation and associated address calculation every 160 ns.

- Parallel/pipeline Harvard architecture
- 3 data-bus structure
- 3 data types : 16-bit real, 32-bit real
  : 16 + 16-bit complex number
- External ROMs
- Pipeline complex multiplier
- 2 x 128 x 16-bit RAM
- 512 x 16-bit coefficient ROM
  32-bit instruction bus
- 64 k x 32-bit external program space
- 68000 family compatibility
- Dual external buses : local/system

HMOS 2

SPECIFICATIONS

PAD LAYOUT	: OAG2
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 8.079 x 7.170mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-229) DIL48



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}*	−0.3 to 7.0	V
Input voltage	V_{IN}*	−0.3 to 7.0	V
Operating temperature range	Toper	0 to 70	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Max. power dissipation	P_D	3	W

* With respect to V_{SS}

ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_{amb} = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input low voltage	V_{IL}	−0.3	–	0.8	V
Input high voltage	V_{IH}	2.4	–	V_{CC}	V
Input leakage current	I_{in}	–	–	10	µA
Output high voltage (I_{load} = −300 µA)	V_{OH}	2.7	–	–	V
Output low voltage (I_{load} = 3.2 mA)	V_{OL}	–	–	0.5	V
Power dissipation	P_D	–	1.5	–	W
Input capacitance	C_{in}	–	10	–	pF
Three state (off state) input current	I_{TSI}	–	–	10	µA

CLOCK AND CONTROL PINS TIMING

Output load 50pF DC characteristics I_{load}

Reference levels: $V_{IL} = V_{OL} = 0.8V$, $V_{IH} = V_{OH} = 2.4V$, tr, tf ≤ 5ns for input signals

Characteristic	Symbol	Min	Typ	Max	Unit
External clock cycle time	tcex	40		160	ns
External clock fall time	tfex			5	ns
External clock rise time	trex			5	ns
EXTAL to CLKOUT high delay	tcoh		25		ns
EXTAL to CLKOUT low delay	tcol		25		ns
CLKOUT rise time	tcor			10	ns
CLKOUT fall time	tcof			10	ns
CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ low	tdsl		5		ns
CLKOUT to DS, RD, WR high	tdsh		5		ns
Control inputs set-up time (BS0...BS2, BE3...BE6, Reset, halt)	tsc	20			ns
Control inputs hold time (BS0...BS2, BE3...BE6, $\overline{Reset}$, $\overline{halt}$)	thc	10			ns
CLKOUT to control output low ($\overline{IRQ}$, BA)	tdlc			50	ns
CLKOUT to control output high (BA)	tdhc			50	ns

LOCAL BUS TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Unit
$\overline{RD}$, $\overline{WR}$, $\overline{AS}$ pulse width	t_{PW}	1/2 tc - 15	–	1/2 tc	ns
address hold time	t_{AH}	10	–	–	ns
data set-up time, write cycle	t_{DSW}	25	–	–	ns
data hold time, write cycle	t_{DHW}	10	–	–	ns
data set-up time, read cycle	t_{DSR}	20	–	–	ns
data hold time, read cycle	t_{DHR}	5	–	–	ns
address valid to $\overline{WR}$, $\overline{AS}$, $\overline{RD}$ low	t_{ARW}	1/2 tc - 40	–	–	ns

INSTRUCTION BUS TIMING

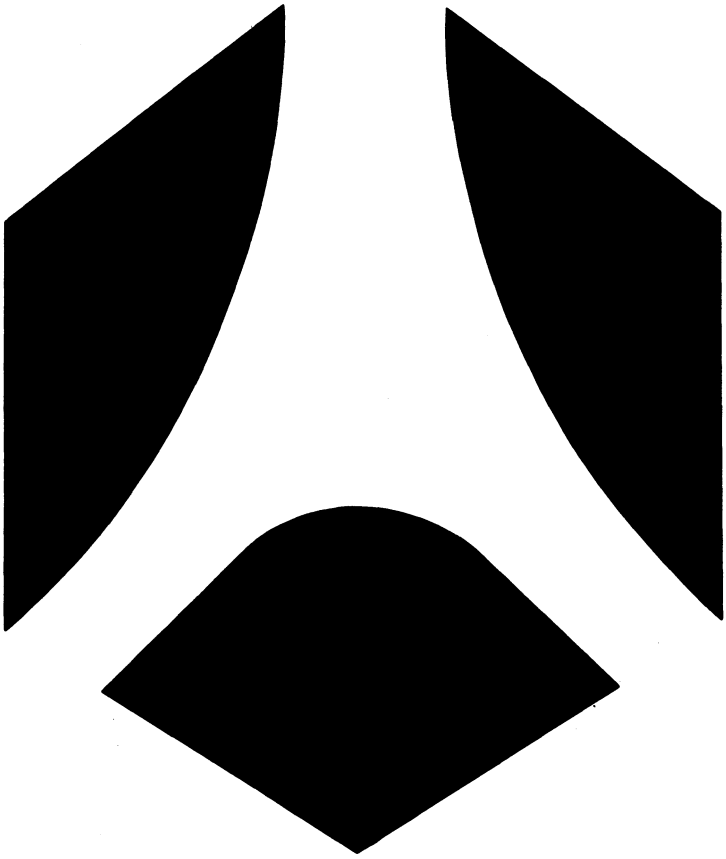
Characteristic	Symbol	Min	Typ.	Max	Unit
CLKOUT high to INCYCLE high	t_{INCH}	5	–	15	ns
CLKOUT low to INCYCLE low	t_{INCL}	5	–	15	ns
CLKOUT high to address valid	t_{IASW}		–	40	ns
I-BUS address hold	t_{IAHW}	20	–	40	ns
Instruction valid	t_{IISR}	20	–		ns
Instruction hold	t_{IIHR}	10	–		ns
CROM data set-up time	t_{DSR}	tc/2 - 40	–		ns
CROM data hold time	t_{DHR}	5	–		ns

SYSTEM BUS TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Unit
$\overline{SDS}$ pulse width	t_{SPW}	60	–	–	ns
SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ set-up time	t_{SAW}	20	–	–	ns
SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ hold after $\overline{SDS}$ high	t_{SAH}	5	–	–	ns
data set-up time, read cycle	t_{SDSR}	20	–	–	ns
data hold time, read cycle	t_{SDHR}	5	–	–	ns
data set-up time, write cycle	t_{SDSW}	–	–	35	ns
data hold time, write cycle	t_{SDHW}	10	–	50	ns
$\overline{SDS}$ low to $\overline{DTACK}$ low	t_{DSLDT}	–	–	50	ns
$\overline{SDS}$ high to $\overline{DTACK}$ high*	t_{DSHDT}	–	–	50	ns
$\overline{SDS}$ high to $\overline{IRQ}$ high	t_{DSHIR}			50	ns

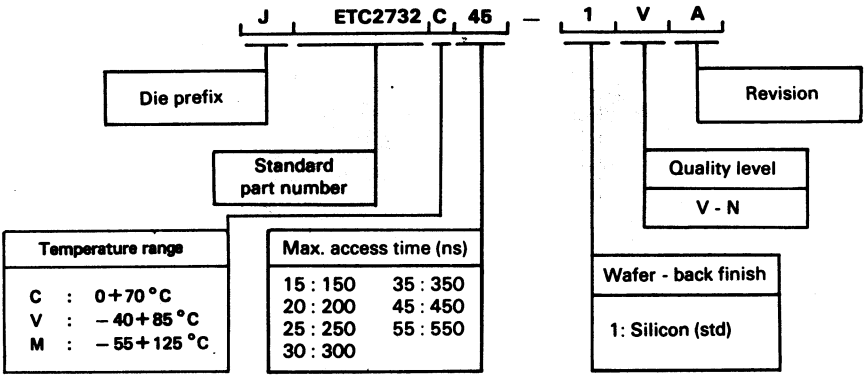
* DTACK is an open drain output test load include $R_L = 820\ \Omega$ at V_{CC}

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.



MOS memories

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
		V	N				1		
J ET2716		X	X				X		A
J ETC2716		X	X				X		A
J ETC2732		X	X				X		A
J TS27C64		X	X				X		A
J TS27C256		X	X				X		A

Part number	Max. access time (ns)						
	15	20	25	30	35	45	55
J ET2716					X	X	
J ETC2716					X	X	X
J ETC2732					X	X	X
J TS27C64	X	X	X	X			
J TS27C256	X	X	X	X			

THOMSON COMPONENTS SEMICONDUCTEURS

J ET2716

16, 384-BIT (2048x8) UV ERASABLE PROM

The ET2716 is a high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

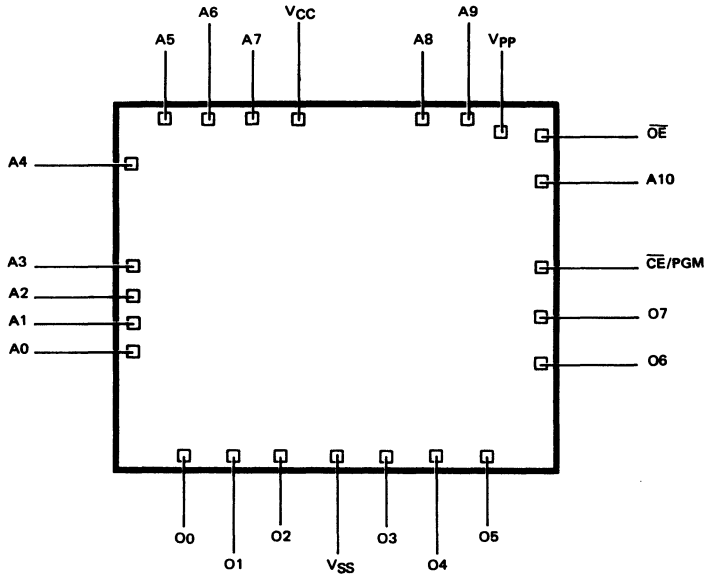
This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

- 2048 x 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time 350 or 450 ns
- Single 5V power supply
- Static-no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- Three-state output with OR-tie capability

NMOS

SPECIFICATIONS

PAD LAYOUT	:	16F
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	3.734 x 3.226mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	DIL24



Back side bias : V_{SS}

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MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply voltage (Note 2)	V_{CC}	− 0.3 to + 6.0	V
Input voltage range (Except V_{pp}) (Note 2)	V_{IN}	− 0.3 to + 6.0	V
Program supply voltage	V_{pp}	− 0.3 to + 26.5	V
Output voltage	V_O	− 0.3 to + 6.0	V
Maximum power dissipation	P_D		W
Programming		1.88	
Operating		1.5	

NOTES :

1— The lid shall be transparent to permit ultraviolet Mlight erasure.
2— Under maximum ratings, voltage values are with respect to ground unless otherwise specified. Throughout the remainder of this data sheet voltage values are with respect to ground.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 10 s.)	T_{lead}	+ 300	°C
Junction-case thermal resistance	$R_{th(j-c)}$	+ 30	°C/W
Junction temperature	T_j	+ 160	°C
Operation case temperature (Note)	T_{oper}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 125	°C

NOTE : The device will be functional at 125°C. However, sustainer operation above 100°C will reduce data retention time.

ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

V_{CC} = 5.3 V, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Output leakage current (chip disable) (Note 2) V_{IH} = 1.95 V, V_{IL} = 0.85 V, V_O = 5.3 V, $\overline{CE}$ = 1.95 V	I_{CEX}	–	–	8	µA
High level input current	I_{IH}				µA
Parallèle : V_{IH} = 5V, V_{IN} = 0		–	–	1	
Serie : V_{IL} = 5.3 V		–	–	1	
Low level input current	I_{IL}				µA
Parallele : V_I = 5.3 V		–	–	1	
Serie : V_I = 0		–	–	1	

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5.3 V, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Standby supply current (Note 3) V_{CC} = 5.5 V, V_{IH} = 1.95 V, V_{IL} = 0.85 V $\overline{CE}$ = 1.95 V, $\overline{OE}$ = 1.95 V, outputs = open	$I_{CC(sb)}$	–	–	22.4	mA
Program current (Note 3) V_{pp} = 5.9 V, V_{IH} = 1.95 V, V_{IL} = 0.85 V	I_{pp}	–	–	4.7	mA
Chip enable to output delay (Note 4) V_{CC} = 4.75 V to 5.25 V, V_{pp} = 4.75 V, V_{IH} = 3.0 V	t_{CE}	4	–	400	ns
Address to output delay (Note 4) V_{CC} = 4.75 V to 5.25 V, $\overline{CE}$ = V_{IL}	t_{ACC}	4	–	400	ns
Output enable to output delay (Note 4) V_{CC} = 4.75 V to 5.25 V, $\overline{CE}$ = V_{IL}	t_{OE}	4	–	200	ns
Input capacitance (Note 5) V_I = 0 V, f = 1.0 MHz	C_I	–	–	6	pF
Output capacitance V_O = 0 V, f = 1.0 MHz	C_O	–	–	12	pF

NOTES :

1– V_{CC} must be applied at the same time or before V_{pp} and remove after or at the same time as V_{pp}.

2– Connect all address inputs and the $\overline{CE}$ input to V_{IH} and measure I_{CEX} with the output under test connected through a current meter to the voltage specified.

3– V_{pp} may be directly connected to V_{CC} except during programming the supply current would then be a sum of I_{CC} and I_{pp}.

4– Output load: TTL gate and C_L = 100 pF ; T_r and T_F < 20 ns
Input pulses level : 0.8 V and 2.2 V ; Input reference level : 1.0 V and 2.0 V. Output timing reference level : 0.8 V and 2.0 V.

5– Capacitance is guaranteed by periodic testing.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit.
Supply voltage	V_{CC} V_{SS}	+ 4.5 to + 5.5 0	V
Program supply voltage (Note)	V_{PP}	V_{CC}	V
Minimum high level input voltage	V_{IH}	+ 2.0 to + 6.5	V
Maximum low level input voltage	V_{IL}	– 0.1 to + 0.8	V
High level programming voltage		+ 24 to + 26	V
Operating temperature	T_{oper}	– 55 to + 125	°C

NOTE : Output load : TTL gate and C_L = 100 pF ; Tr and T_f < 20 ns.
Input pulses level : 0.8 V and 2.2 V ; Input reference level : 1.0 V and 2.0 V ; Output timing reference level 0.8 V and 2.0 V.

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J ETC2716

16, 384-BIT (2048x8) UV ERASABLE PROM

The ETC2716 is a high speed 16K UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around pattern experimentation and low power consumption are important requirements.

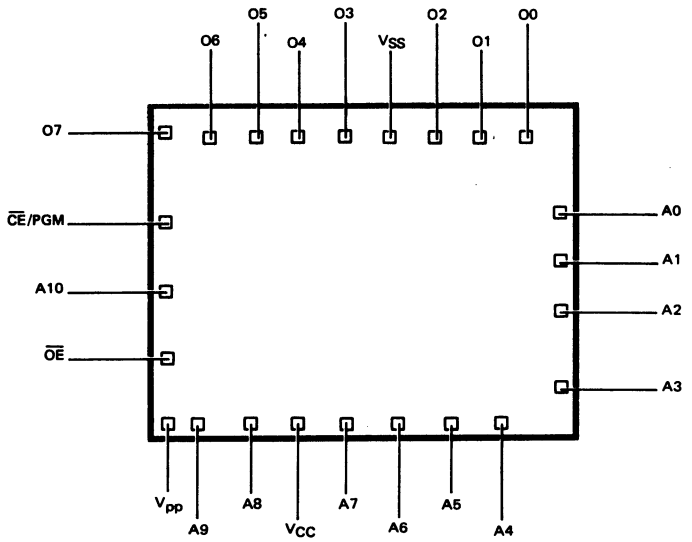
This EPROM is fabricated with the reliable, high volume, time proven, P2CMOS silicon gate technology.

- CMOS power consumption
- Performance compatible to market standard 8-bit CMOS Microp
- 2048 x 8 organization
- Pin compatible to 2716
- Access time 350 ns, 450 ns or 550 ns
- Single 5V power supply
- Static - no clocks required
- TTL compatible I/Os during both read and program modes
- Three-state output with OR-tie capability

CMOS

SPECIFICATIONS

PAD LAYOUT	:	C166
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	4.38 x 3.47mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	DIL24



Back side bias : V_{SS}

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MAXIMUM RATING (Note)

Rating	Symbol	Value	Unit
Program supply voltage	V_{pp}	− 0.6 to + 14	V
Inputs voltage A9 (except V_{pp})	V_{IN}	− 0.6 to + 13.5	V
Inputs voltage V_{pp} A9		− 0.6 to + 6.25	V
Maximum power dissipation Programming Operating	P_D	 — 1.0	W

NOTE : "MAXIMUM RATINGS" are those values beyond which the safety of the device cannot be guarranted. They are not meant to imply that the devices should be operated at theses limits. The table of electrical characteristics provides conditions for actual device operation.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 10 s.)	T_{lead}	+ 300	°C
Junction temperature	T_j	+ 160	°C
Operation case temperature (Note)	T_{oper}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 125	°C

NOTE : The device will be functional at 125°C. However, sustainer operation above 100°C will reduce data retention time.

ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = 5\ V \pm 5\ \%$, $T_{amb} = 25°C$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Supply active current - TTL levels Data in = 0.8, 2.2 V - Data out = open $\overline{CE} = \overline{OE} = V_{IL}$, $V_{CC} = 5.3\ V$, $F = 1\ MHz$	I_{CC1}	—	—	10	mA
Supply active current - MOS levels Data in = 0, 5.3 V - Data out = open $\overline{CE} = \overline{OE} = 0\ V$; $V_{CC} = 5.3\ V$, $F = 1\ MHz$	I_{CC2}	—	—	5	mA
Supply standby current - TTL levels Data in = $\overline{OE} = V_{IL}$ - Data out = open $\overline{CE} = 2.2\ V$, $V_{pp} = V_{CC} = 5.3\ V$	$I_{CC(sb)1}$	—	—	900	µA

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5 V ± 5 %, T_{amb} = 25°C (unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit.
Standby supply current - MOS levels Data in = $\overline{OE}$ = GND - Data out = open $\overline{CE}$ = 5.3 V, V_{pp} = V_{CC} = 5.3 V		$I_{CC(sb)2}$	–	–	90	µA
V_{pp} read current Data in = V_{IL} - Data out = open $\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{CC} = 5.3 V		I_{pp}	–	–	9	µA
Output leakage current - COLEAK Data in = V_{IL}, V_{pp} = V_{CC} = 5.3 V $\overline{OE}$ = 0.8 V, $\overline{CE}$ = 2.2 V, V_{OH} = 5.3 V		I_{CEX1}	–	–	6	µA
Output leakage current - PROGLEAK Data in = V_{IL} - Data out = 5.3 V or VSS $\overline{CE}$ = 0.8 V, $\overline{OE}$ = 2.2 V, V_{pp} = 26 V, V_{CC} = 5.3 V		I_{CEX2}	–	–	6	µA
Input leakage current Data out = open, V_{pp} = V_{cc} = 5.3 V V_I = 5.3 V or V_{SS}		I_I	–	–	1	µA
Low level input voltage		V_{IL}	– 0.1	–	0.8	V
High level input voltage		V_{IH}	2.0	–	V_{CC} + 1	V
Low level output current V_{CC} = V_{pp} = 4.7 V	TTL (V_{OL} = 0.45 V) MOS (V_{OL} = 0.1 V)	I_{OL}	– –	– –	2.1 0	mA
High level output current V_{CC} = V_{pp} = 4.7 V	TTL (V_{OH} = 2.4 V) MOS (V_{OH} = 4.65 V)	I_{OH}	– 500 0	– –	– –	µA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit.
Supply voltage	V_{CC}	5 ± 5 %	V
Minimum high level input voltage	V_{IH}	+ 2.0 to + 6.5	V
Maximum low level input voltage	V_{IL}	– 0.1 to + 0.8	V
High level programming voltage		+ 12.2 to + 12.8	V
Operating temperature	T_{oper}	– 55 to + 125	°C

THOMSON COMPONENTS SEMICONDUCTEURS

J ETC2732

32, 768-BIT (4096x8) UV ERASABLE PROM

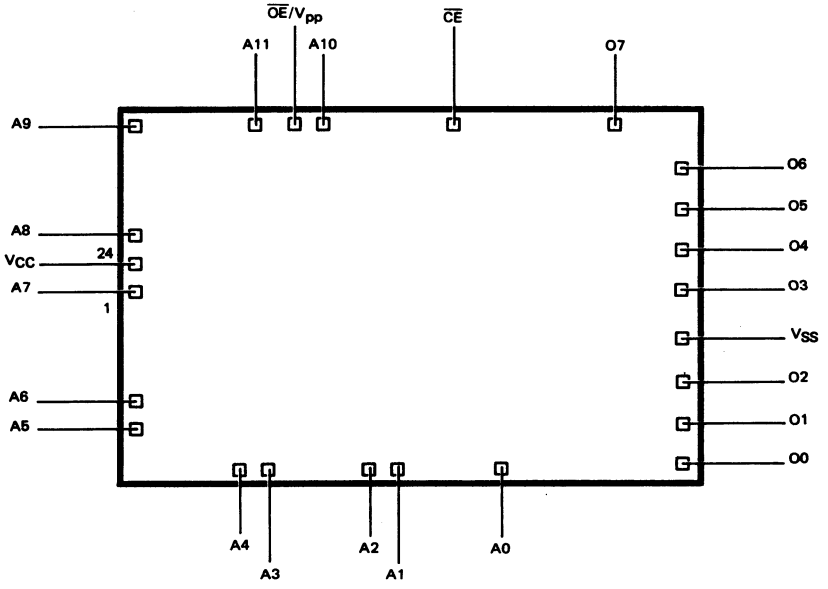
The ETC2732 is a high speed 32K UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

- CMOS power consumption : 26.25 mW max active power, 0.53 mW max standby power
- 4096 x 8 organization
- Access time 350 ns, 450 ns or 550 ns
- Single 5V power supply
- Static - no clocks required
- TTL compatible I/Os during both read and program modes
- Three-state output with OR-tie capability

CMOS

SPECIFICATIONS

PAD LAYOUT	:	C32A
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	5.54 x 3.61mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	DIL24



Back side bias : V_{SS}

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MAXIMUM RATINGS (Note)

Rating	Symbol	Value	Unit
Program supply voltage	V_{pp}	− 0.6 to + 14	V
Inputs voltage A9 (except V_{pp})	V_{IN}	− 0.6 to + 13.5	V
Inputs voltage V_{pp} A9		− 0.6 to + 6.25	V
Maximum power dissipation Programming Operating	P_D	 – 1.0	W

NOTE : "MAXIMUM RATINGS" are those values beyond which the safety of the device cannot be guarranted. They are not meant to imply that the devices should be operated at theses limits. The table of electrical characteristics provides conditions for actual device operation.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 10 s.)	T_{lead}	+ 300	°C
Junction temperature	T_j	+ 160	°C
Operation case temperature (Note)	T_{oper}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 125	°C

NOTE : The device will be functional at 125°C. However, sustainer operation above 100°C will reduce data retention time.

ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = 5\ V \pm 5\ \%$, $T_{amb} = 25°C$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Supply active current - TTL levels Data in = 0.8, 2.2 V - Data out = open $\overline{CE} = \overline{OE} = V_{IL}$, $V_{CC} = 5.3\ V$, F = 1 MHz	I_{CC1}	–	–	10	mA
Supply active current - MOS levels Data in = 0, 5.3 V - Data out = open $\overline{CE} = \overline{OE} = 0\ V$; $V_{CC} = 5.3\ V$, F = 1 MHz	I_{CC2}	–	–	5	mA
Supply standby current - TTL levels Data in = $\overline{OE} = V_{IL}$ - Data out = open $\overline{CE} = 2.2\ V$, $V_{pp} = V_{CC} = 5.3\ V$	$I_{CC(sb)1}$	–	–	1	mA

ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = 5\ V \pm 5\ \%$, $T_{amb} = 25°C$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Standby supply current - MOS levels Data in = $\overline{OE}$ = GND - Data out = open $\overline{CE} = 5.3\ V$, $V_{CC} = 5.3\ V$	$I_{CC(sb)2}$	–	–	100	µA
Output leakage current - COLEAK Data in = V_{IL}, $V_{CC} = 5.3\ V$ $\overline{OE} = 0.8\ V$, $CE = 2.2\ V$, $V_{OH} = 5.3\ V$	I_{CEX1}	–	–	6	µA
Output leakage current - PROGLEAK Data in = V_{IL} - Data out = 5.3 V or V_{SS} $\overline{CE} = 0.8\ V$, $OE = 2.2\ V$, $V_{pp} = 26\ V$, $V_{CC} = 5.3\ V$	I_{CEX2}	–	–	6	µA
Input leakage current Data out = open, $V_{CC} = 5.3\ V$ VI = 5.3 V or V_{SS}	I_I	–	–	1	µA
Low level input voltage	V_{IL}	– 0.1	–	0.8	V
High level input voltage	V_{IH}	2.0	–	$V_{CC} + 1$	V
Low level output current (TTL) $V_{CC} = V_{pp} = 4.7\ V$, $V_{OL} = 0.45\ V$	I_{OL}	–	–	2.1	mA
High level output current (TTL) $V_{CC} = V_{pp} = 4.7\ V$, $V_{OH} = 2.4\ V$	I_{OH}	– 500	–	–	µA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit.
Supply voltage	V_{CC}	$5 \pm 5\ \%$	V
Minimum high level input voltage	V_{IH}	+ 2.0 to + 6.5	V
Maximum low level input voltage	V_{IL}	– 0.1 to + 0.8	V
High level programming voltage		+ 12.2 to + 12.8	V
Operating temperature	T_{oper}	– 55 to + 125	°C

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS27C64

65, 536-BIT (8192x8) UV ERASABLE PROM

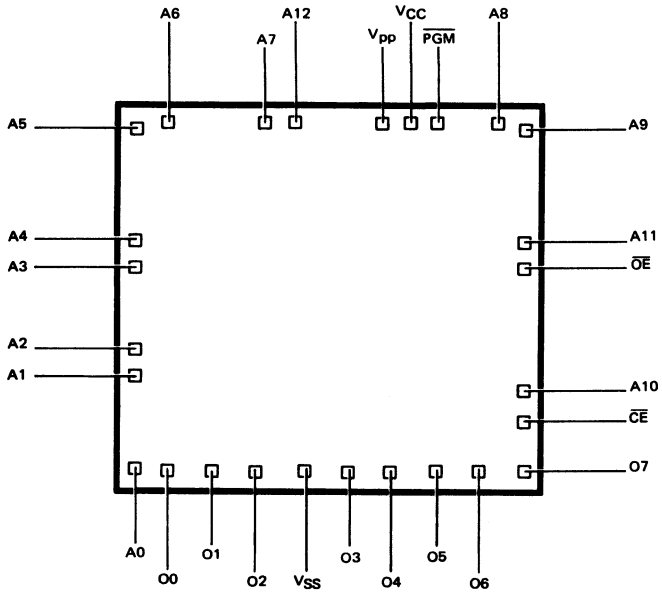
The TS27C64 is a high speed 64K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and patterne experimentation are important requirements.

- Fast Access time – 150ns, 200ns, 250ns, 300ns
- Compatible to high speed microprocessors zero wait state
- Low power consumption : active 20 mA (max.)
  standby 1 mA (max.)
- Programming voltage : 12.5 V
- High speed programming (< 1 minute)
- Electronic signature

CMOS

SPECIFICATIONS

PAD LAYOUT	: C64C
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 3.17 x 2.87mm
DIE THICKNESS	: 0.50mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: DIL28



Back side bias : V_{SS}

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MAXIMUM RATINGS (Note)

Rating	Symbol	Value	Unit
Program supply voltage	V_{PP}	− 0.6 to + 14	V
Inputs voltage A9 (except V_{PP})	V_{IN}	− 0.6 to + 13.5	V
Inputs voltage V_{PP} A9		− 0.6 to + 6.25	V
Maximum power dissipation Programming Operating	P_D	 − 1.5	W

NOTE : "MAXIMUM RATINGS" are those values beyond which the safety of the device cannot be guarranted. They are not meant to imply that the devices should be operated at theses limits. The table of electrical characteristics provides conditions for actual device operation.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 10 s.)	T_{lead}	+ 300	°C
Junction temperature	T_j	+ 160	°C
Operation case temperature (Note)	T_{oper}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 125	°C

NOTE : The device will be functional at 125°C. However, sustainer operation above 100°C will reduce data retention time.

ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = 5\ V \pm 5\ \%$, $T_{amb} = 25°C$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Supply active current - TTL levels Data out = open, $\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$, $V_{CC} = 5.6\ V$	I_{CC}	−	−	5	mA
Supply standby current - TTL levels Data out = open, $\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$, $V_{CC} = 5.6\ V$	$I_{CC(sb)}$	−	−	1.5	mA
V_{PP} read current Data in = V_{IH} - Data out = open $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, $V_{CC} = 5.6\ V$	I_{pp}	−	−	5	mA

ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = 5\ V \pm 5\ \%$, $T_{amb} = 25°C$ (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Output leakage current $V_{pp} = V_{CC} = V_{SS}$, $\overline{OE} = V_{IL}$ $\overline{CE} = V_{IH}$, $V_I = 5.6\ V$ or V_{SS}	I_{CEX}	–	–	10	µA
Input leakage current Data out $= V_{pp} = V_{CC} = V_{SS}$ $V_I = 5.6\ V$ or V_{SS}	I_I	–	–	10	µA
Low level input voltage	V_{IL}	– 0.1	–	0.8	V
High level input voltage $V_O = V_{pp} = V_{CC} = V_{SS}$	V_{IH}	2.0	–	$V_{CC} + 1$	V
Low level output current $V_{CC} = V_{pp} = 4.5\ V$, $V_{OL} = 0.4\ V$	I_{OL}	–	–	2.1	mA
High level output current $V_{CC} = V_{pp} = 4.5\ V$, $V_{OH} = 2.4\ V$	I_{OH}	400	–	–	µA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit.
Supply voltage	V_{CC}	$5 \pm 5\ \%$	V
Minimum high level input voltage	V_{IH}	+ 2.0 to + 6.5	V
Maximum low level input voltage	V_{IL}	– 0.1 to + 0.8	V
High level programming voltage		+ 12.2 to + 12.8	V
Operating temperature	T_{oper}	– 55 to + 125	°C

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.

THOMSON COMPONENTS SEMICONDUCTEURS

J TS27C256

262, 144-BIT (32,768x8) UV ERASABLE PROM

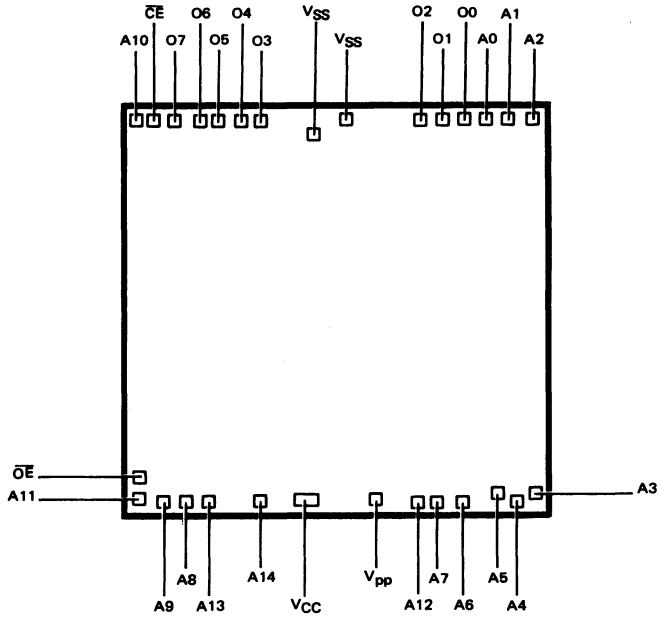
The TS27C256 is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

- Fast access time – 150ns, 200ns, 250ns, 300ns
- Compatible to high speed microprocessors zero wait state
- Low power consumption : active 40 mA (max.)
  standby 1 mA (max.)
- Programming voltage : 12.5 V
- High speed programming
- Electronic signature

CMOS

SPECIFICATIONS

PAD LAYOUT	:	C256V1
PAD SIZE	:	0.1 x 0.1mm
DIE SIZE	:	5.36 x 5.18mm
DIE THICKNESS	:	0.50mm
METALLIZATION	:	Al (front side)
PASSIVATION	:	Pyrolitic oxide
REVISION	:	A
QUALIFICATION		
LOT CASE	:	DIL28



Back side bias : V_{SS}

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MAXIMUM RATINGS (Note)

Rating	Symbol	Value	Unit
Program supply voltage	V_{pp}	− 0.6 to + 14	V
Inputs voltage A9 (except V_{pp})	V_{IN}	− 0.6 to + 13.5	V
Inputs voltage V_{pp} A9		− 0.6 to + 6.25	V
Maximum power dissipation Programming Operating	P_D	 – 1.0	W

NOTE : "MAXIMUM RATINGS" are those values beyond which the safety of the device cannot be guarranted. They are not meant to imply that the devices should be operated at theses limits. The table of electrical characteristics provides conditions for actual device operation.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 10 s.)	T_{lead}	+ 300	°C
Junction temperature	T_j	+ 160	°C
Operation case temperature (Note)	T_{oper}	− 55 to + 125	°C
Storage temperature	T_{stg}	− 65 to + 125	°C

NOTE : The device will be functional at 125°C. However, sustainer operation above 100°C will reduce data retention time.

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5 V ± 5 %, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Supply active current - TTL levels Data in = 0 or 5 V - Data out = open $\overline{CE} = \overline{OE} = 0$ V, $V_{pp} = V_{CC} = 5.25$ V, F = 5 MHz	I_{CC}	–	–	32	mA
Supply standby current - TTL levels Data in = V_{IH} - Data out = open $\overline{CE} = \overline{OE} = V_{IH}$; $V_{CC} = 5.6$ V	$I_{CC(sb)}$	–	–	1	mA
V_{pp} read current Data in = 0 V - Data out = open $\overline{CE} = \overline{OE} = 0$ V, $V_{CC} = 5$ V	I_{pp}	–	–	100	µA

ELECTRICAL OPERATING CHARACTERISTICS

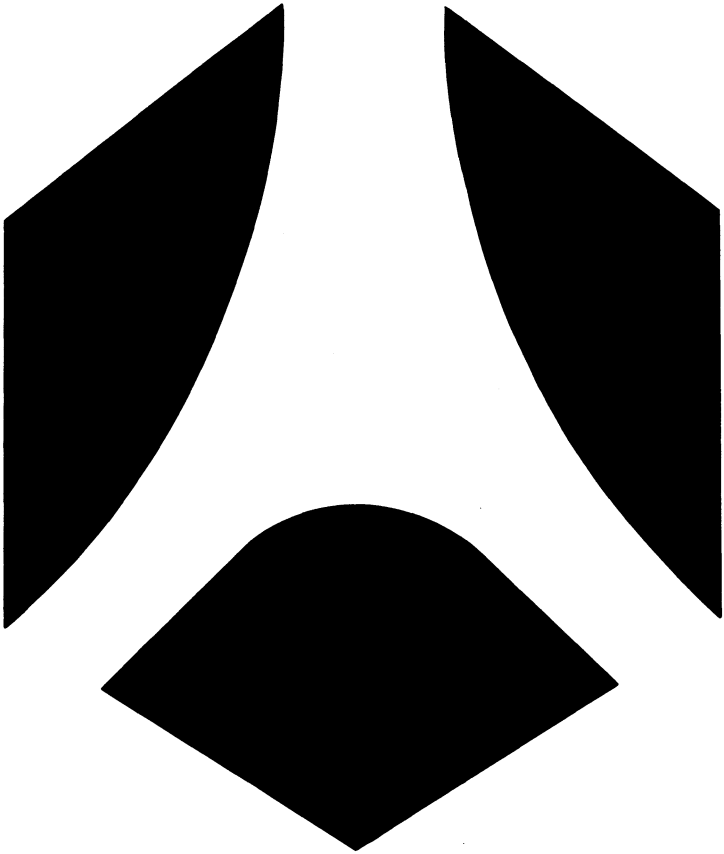
V_{CC} = 5 V ± 5 %, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Output leakage current $V_{pp} = V_{CC} = V_{SS}$, Data in = V_{IL} $\overline{OE} = \overline{CE} = V_{IH}$, V_I = 5.6 V or V_{SS}	I_{CEX}	–	–	10	µA
Input leakage current Data out = $V_{pp} = V_{CC} = V_{SS}$ V_I = 5.6 V or V_{SS}	I_I	–	–	10	µA
Low level input voltage	V_{IL}	– 0.1	–	0.8	V
High level input voltage $V_O = V_{pp} = V_{CC} = V_{SS}$	V_{IH}	2.0	–	V_{CC} + 1	V
Low level output voltage $V_{CC} = V_{pp}$ = 4.5 V, I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
High level output voltage $V_{CC} = V_{pp}$ = 5 V,	V_{OH}	2.4	–	–	V
Low level output current $V_{CC} = V_{pp}$ = 5 V, V_{OL} = 0.45 V	I_{OL}	–	–	2.1	mA
High level output current $V_{CC} = V_{pp}$ = 5 V ; V_{OH} = 2.4 V	I_{OH}	– 400	–	–	µA

RECOMMENDED OPERATING CONDITIONS

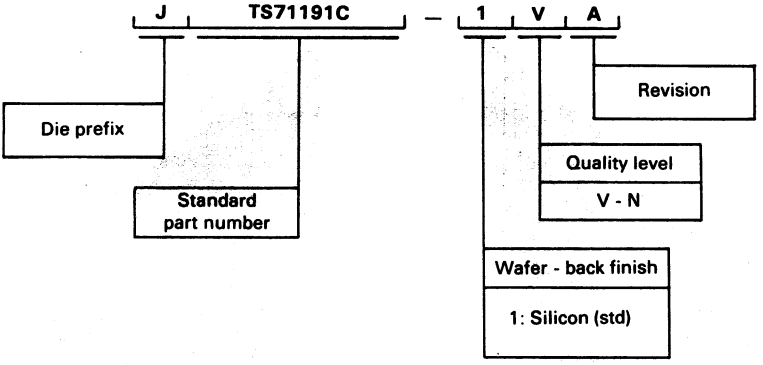
Characteristic	Symbol	Value	Unit.
Supply voltage	V_{CC}	5 ± 5 %	V
Minimum high level input voltage	V_{IH}	+ 2.0 to + 6.5	V
Maximum low level input voltage	V_{IL}	– 0.1 to + 0.8	V
High level programming voltage		+ 12.2 to + 12.8	V
Operating temperature	T_{oper}	– 55 to + 125	°C

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.



Bipolar memories

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	1	2	
J TS71191C		X	X				X		A

THOMSON COMPONENTS SEMICONDUCTEURS

J TS71191C

16 K FAST PROM

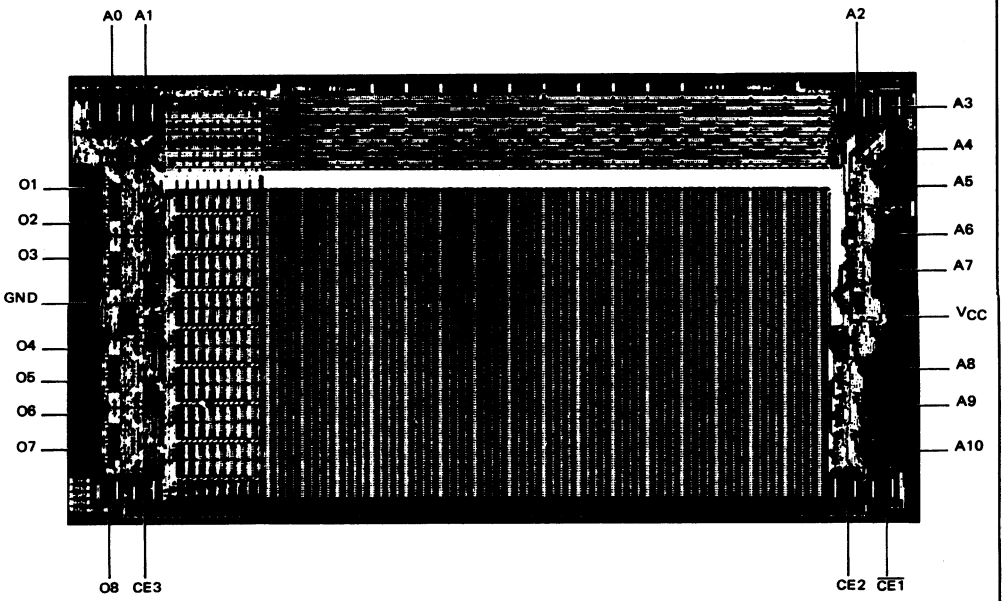
The TS71191C is programmable read-only memorie (PROM) organized in a 2048 words by 8-bit configuration and is field programmable. It is shipped in an unprogrammed form and has "0" in all locations.

- Fast access time : 35 ns max
- Temperature compensating circuits to achieve a wide range of operation
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology
- TTL compatible

BIPOLAR

SPECIFICATIONS

PAD LAYOUT	: L033
PAD SIZE	: 0.1 x 0.1mm
DIE SIZE	: 4.63 x 2.42mm
DIE THICKNESS	: 0.5mm
METALLIZATION	: Al (front side)
PASSIVATION	: Pyrolitic oxide
REVISION	: A
QUALIFICATION	
LOT CASE	: (CB-68) DIL24



Back side bias : $V_{\overline{CC}}$

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power supply	V_{CC}	5 ± 5 %	V
Supply voltage to ground potential continuous		− 0.5 to + 7.0	V
Voltage applied to outputs Except during programming During programming	V_O	− 0.5 to V_{CC} max.	V
Output current into outputs during programming (max. duration of 1 s.)	I_O	550	mA
Input voltage range	V_{IN}	− 0.5 to V_{CC} max	V
Input current	I_I	− 30 to + 5	mA
Output sink current (note 1)	$I_{O\ (sink)}$	100	mA
Maximum power dissipation (note 2)	P_D	1.02	W

NOTES :
1— Heat sinking is recommended to reduce junction temperature
2— Must with stand the added P_D due to short circuit test (E.G. I_{OS})

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Lead temperature (soldering 5 s.)	T_{lead}	270	°C
Temperature (ambiant) under bias	T_{amb}	− 55 to + 125	°C
Maximum junction temperature	T_j	175	°C
Storage temperature	T_{stg}	− 65 to + 165	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 5.5 V, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Supply current Outputs = grounded, V_O = 0 V	I_{CC}	—	—	185	mA
Low level input voltage (Note 1)	V_{IL}	0.8	—	—	V
High level input voltage (Note 1)	V_{IH}	—	—	2.5	V

NOTES :
1— Parameters no specified in MIL 38510
2— Theses parameters are not 100 % tested.

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 5.5 V, T_{amb} = 25°C (unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit.
Low level input current V_I = 0.45 V	I_{IL}	–	–	– 250	µA
High level input current V_{IH} = 5.5 V	I_{IH}	–	–	50	µA
Maximum input current at V_{IH} min (Note 1) V_{CC} = V_{CC} max, V_I = 2.7 V	I_I	–	–	NT	µA
Input clamp voltage V_{CC} = 4.5 V, I_{IN} = – 18 mA	V_{IC}	–	–	– 1.2	V
Low level output voltage V_{CC} = 4.5 V, V_I = V_{IH} or V_{IL}, I_{OL} = 16 mA	V_{OL}	–	–	0.5	V
High level output voltage V_{CC} = 4.5 V, V_I = V_{IH} or V_{IL}, I_{OH} = 2 mA	V_{OH}	2.4	–	–	V
High impedance (off-state) output low current V_O = 0.5 V	I_{OZL}	–	–	– 60	µA
High impedance (off-state) output high current $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V, V_O = 5.5 V	I_{OZH}	–	–	60	µA
Short circuit output current (Note 2)	I_{OS}	– 15	–	– 85	mA
Chip enable to output delay $\overline{CE1}$, CE2, CE3 to Q1 – Q8	t_{CE}	5	–	50	ns
Address to output delay (A0-A10 to Q1-Q8) V_{CC} = 4.5 V and 5.5 V, C_L = 30 pF	t_{ACC}	5	–	100	ns
Input capacitance (Note 2) V_I = 2V, F = 1 MHz	C_I	–	–	5	pF
Output capacitance (Note 2) V_I = 2 V, F = 1 MHz	C_O	–	–	8	pF

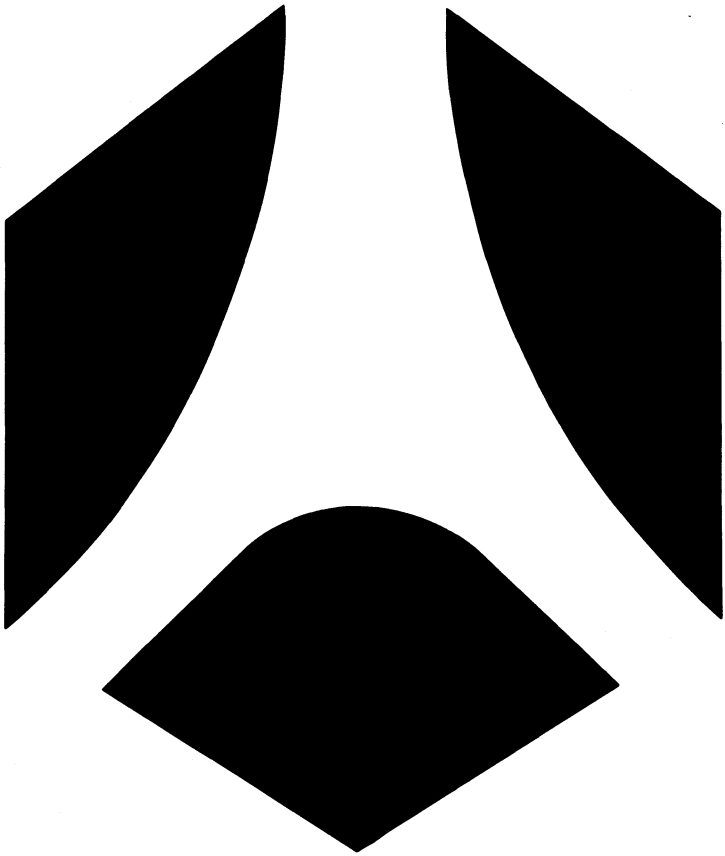
NOTES :

1– Parameters no specified in MIL 38510
2– Theses parameters are not 100 % tested.

RECOMMENDED OPERATING CONDITIONS

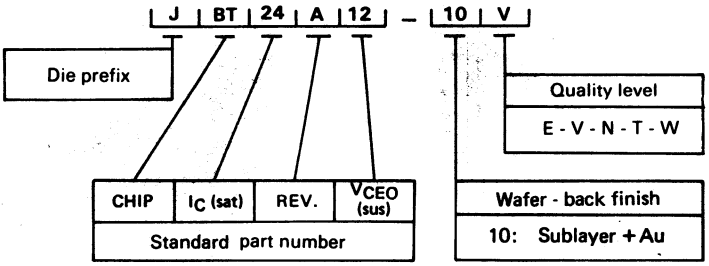
Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
Minimum high level input voltage	V_{IH}	+ 2.0	V
Maximum low level input voltage	V_{IL}	+ 0.8	V
Normalized fanout (each output)		16	mA
Operating temperature	T_{oper}	– 55 to + 125	°C

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different products.



Power transistors

ORDERING INFORMATION



Part number	Quality level						Wafer - back finish		Revision
	E	V	N	T	W	Z	10		
J BT08B12	X	X	X	X	X		X		B
J BT11B12	X	X	X	X	X		X		B
J BT20B12	X	X	X	X	X		X		B
J BT24B12	X	X	X	X	X		X		B
J BT30B12	X	X	X	X	X		X		B
J BT50B12	X	X	X	X	X		X		B
J BT60B12	X	X	X	X	X		X		B
J BT06B20	X	X	X	X	X		X		B
J BT10B20	X	X	X	X	X		X		B
J BT25B20	X	X	X	X	X		X		B
J BT40B20	X	X	X	X	X		X		B
J BT05B25	X	X	X	X	X		X		B
J BT08B25	X	X	X	X	X		X		B
J BT16B25	X	X	X	X	X		X		B
J BT35B25	X	X	X	X	X		X		B
J BT10B30	X	X	X	X	X		X		B
J BT30B30	X	X	X	X	X		X		B
J BT02B45	X	X	X	X	X		X		B
J BT05B45	X	X	X	X	X		X		B
J BT08B45	X	X	X	X	X		X		B
J BT12B45	X	X	X	X	X		X		B
J BT16B45	X	X	X	X	X		X		B

THOMSON COMPONENTS SEMICONDUCTEURS

J BTO8B12

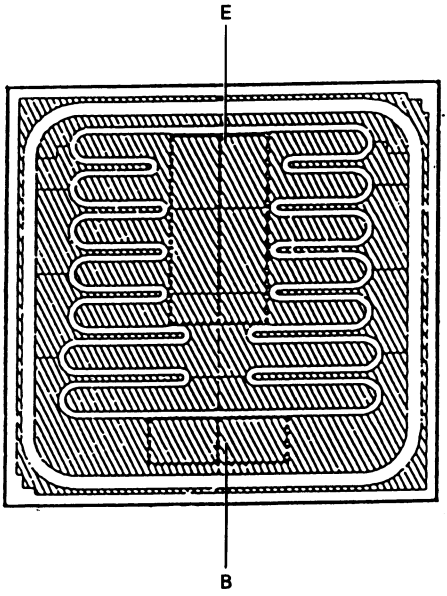
FAST NPN SWITCHING TRANSISTOR

High speed transistor suited for low voltage applications.
High frequency and efficiency converters switching regulators motor control.

SUPERSWITCH

SPECIFICATIONS

MASK	: 318
DIE SIZE	: 3.17 x 3.17mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Sublayer + Au (back side)
PASSIVATION	: Thermal oxide
PRODUCT ISSUE	: BUV26
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	90	V
Collector-base voltage	V_{CBO}	180	V
Emitter-base voltage	V_{EBO}	7	V
Collector current	I_C I_{CM}	14 25	A
Base current	I_B I_{BM}	4 6	A
Junction temperature	T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	100	–	–	V
Collector - emitter cut-off current $V_{CE} = 180$ V, $V_{BE} = 0$ $R_{BE} = 50\ \Omega$	 I_{CES} I_{CER}	 – –	 – –	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	–	–	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1$ A	h_{FE}	–	–	60	–

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 8$ A, $I_B = 0{,}8$ A	$V_{CE\ sat}$	–	–	1.5	V
Base-emitter saturation voltage $I_C = 8$ A, $I_B = 0{,}8$ A	V_{BEsat}	–	–	2	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT08B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT11B12

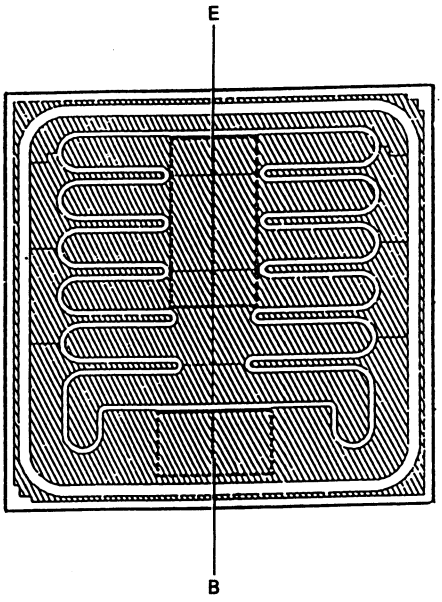
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 319
DIE SIZE	: 3.78 x 3.78mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW90
QUALIFICATION LOT CASE	: TO3



April 1987-1/2

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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	125	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	250	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	20 30	A
Base current		$I_{B(RMS)}$ I_{BM}	4 6	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	100	−	−	V
Collector - emitter cut-off current $V_{CE} = 160$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 11$ A, $I_B = 1.1$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 11$ A, $I_B = 1.1$ A	V_{BEsat}	−	−	1.6	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJB11B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT20B12

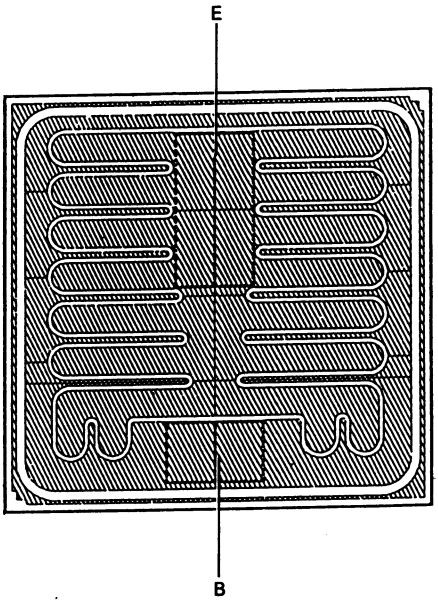
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 317
DIE SIZE	: 4.48 x 4.48mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW50
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	125	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	250	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	25 50	A
Base current		$I_{B(RMS)}$ I_{BM}	6 12	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	125	−	−	V
Collector - emitter cut-off current $V_{CE} = 250$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	0.5	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1$ A	h_{FE}	−	−	70	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 20$ A, $I_B = 2$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 20$ A, $I_B = 2$ A	V_{BEsat}	−	−	1.6	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT20B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT24B12

FAST SWITCHING POWER TRANSISTOR

- Suitable for motor drives, converters SMPS and UPS.
- Mains : Medium voltage supply.

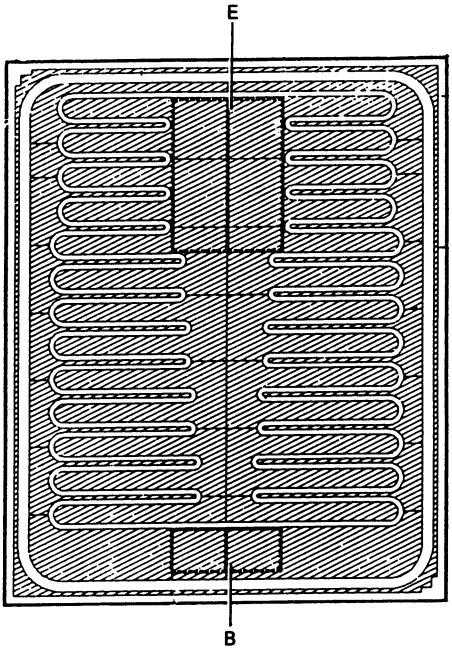
Features

- $\beta_F > 10$ at $I_C = 30$ A.
- High efficiency.
- Very low saturation voltage.
- Rectangular safe operating area.
- Wide accidental overload area.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 320
DIE SIZE	: 5.14 x 4.10mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Sublayer + Au : (front side) : or Ag (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUT60
QUALIFICATION	
LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	125	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	200	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{E(RMS)}$ I_{EM}	16 32	A
Base current		$I_{B(RMS)}$ I_{BM}	5 10	A
Junction temperature		T_j	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	125	–	–	V
Collector - base cut off current $V_{CB} = 200$ V, $I_E = 0$	I_{CBO}	–	–	0.1	mA
Collector-emitter cut-off current $V_{CE} = 200$ V, $R_{BE} = 10\ \Omega$	I_{CER}	–	–	0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	–	–	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 2.5$ A	h_{FE}	–	–	70	–

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 12$ A, $I_B = 0.6$ A	$V_{CE\ sat}$	–	–	0.9	V
Base-emitter saturation voltage $I_C = 12$ A, $I_B = 0.6$ A	V_{BEsat}	–	–	1.3	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT24B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT30B12

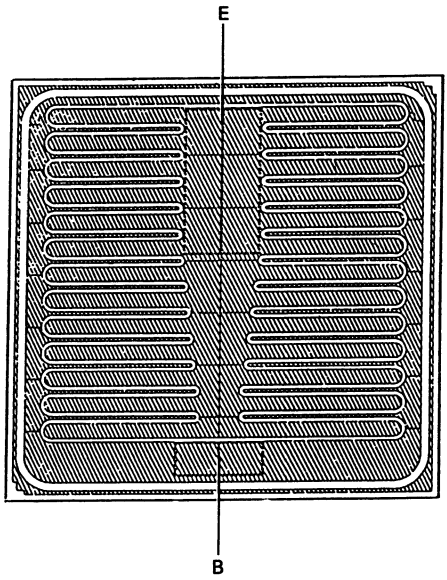
NPN HIGH CURRENT SWITCHING TRANSISTORS

High current, high speed transistor suited for low voltage applications:
- High frequency and efficiency converters.
- Switching regulators.
- Motor controls.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 315
DIE SIZE	: 5.14 x 5.14mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW48
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	60	V
Collector-emitter voltage	V_{CEX}	120	V
Emitter-base voltage	V_{EBO}	7	V
Collector current	I_C I_{CM}	30 45	A
Base current	I_B I_{BM}	8 12	A
Junction temperature	T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	80	−	−	V
Collector - emitter cut-off current $V_{CE} = 160$ V, $V_{BE} = 0$ $R_{BE} =$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 5$ A	h_{FE}	−	−	70	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 15$ A, $I_B = 1.5$ A	$V_{CE\ sat}$	−	−	0.5	V
Base-emitter saturation voltage $I_C = 15$ A, $I_B = 1.5$ A	V_{BEsat}	−	−	1.4	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT30B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT50B12

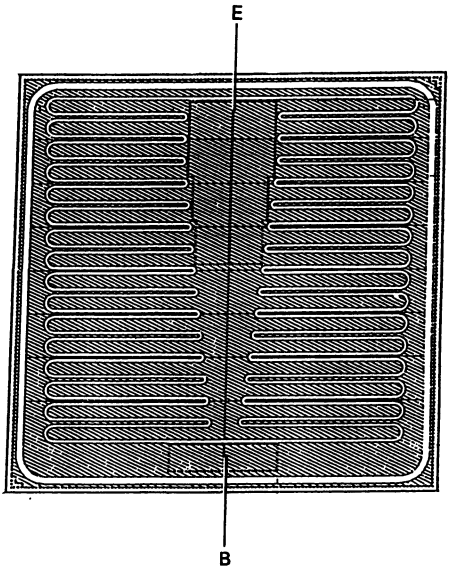
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 316
DIE SIZE	: 6.02 x 6.02mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUV60
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	125	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	250	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	50 80	A
Base current		$I_{B(RMS)}$ I_{BM}	10 18	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	125	–	–	V
Collector - base cut-off current $V_{CB} = 250$ V, $I_E = 0$	I_{CBO}	–	–	0.1	mA
Collector-emitter cut-off current $V_{CE} = 250$ V, $R_{BE} = 40\ \Omega$	I_{CER}	–	–	0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	–	–	1	mA
Forward current gain $V_{CE} = 4$ V, $I_C = 2.5$ A	h_{FE}	–	–	70	–

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 15$ A, $I_B = 1.5$ A	$V_{CE\ sat}$	–	–	0.5	V
Base-emitter saturation voltage $I_C = 20$ A, $I_B = 0.9$ A	V_{BEsat}	–	–	1.3	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS.JBT50B12

THOMSON COMPONENTS SEMICONDUCTEURS

J BT60B12

FAST SWITCHING POWER TRANSISTOR

High current, high speed transistor suited for power conversion applications high efficiency converters motors controls.

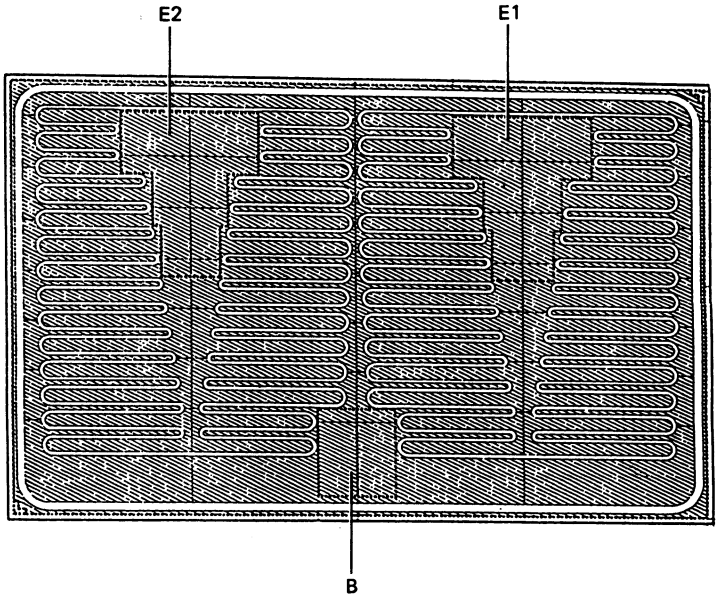
Higher efficiency due to:

- Less base current requirements.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 314
DIE SIZE	: 8.7 x 5.6mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUT90
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	125	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	200	V
Emitter-base voltage		V_{EBO}	10	V
Collector current		$I_{C(RMS)}$ I_{CM}	50 120	A
Base current		$I_{B(RMS)}$ I_{BM}	12 32	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	125	−	−	V
Collector - emitter cut-off current $V_{CE} = 200$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -10$ V $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 2.5$ A	h_{FE}	−	−	75	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 30$ A, $I_B = 3$ A	$V_{CE\ sat}$	−	−	0.6	V
Base-emitter saturation voltage $I_C = 35$ A, $I_B = 1.75$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT60B12

THOMSON COMPONENTS SEMICONDUCTEURS

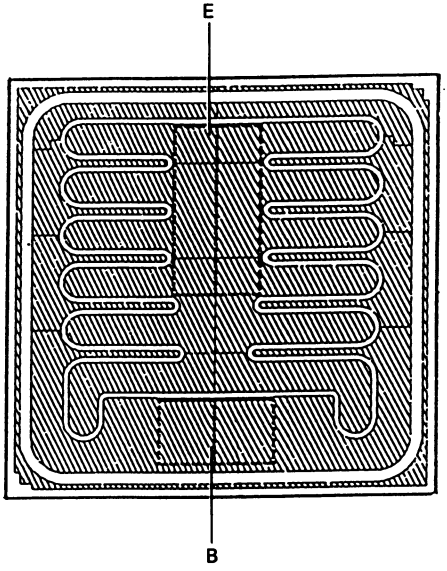
J BT06B20

FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

RACE PROCESS	: 319
DIE SIZE	: 3.78 x 3.78mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side)
	: Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW91
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	200	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	300	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	15 20	A
Base current		$I_{B(RMS)}$ I_{BM}	3 5	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	200	−	−	V
Collector - emitter cut-off current $V_{CE} = 300$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 6$ A, $I_B = 0.6$ A	$V_{CE\ sat}$	−	−	0.9	V
Base-emitter saturation voltage $I_C = 6$ A, $I_B = 0.6$ A	V_{BEsat}	−	−	0.6	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT06B20

THOMSON COMPONENTS SEMICONDUCTEURS

J BT10B20

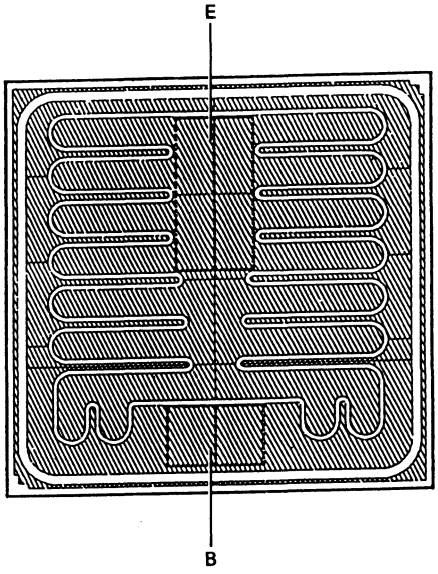
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 317
DIE SIZE	: 4.48 x 4.48mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW51
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	200	V
Collector-emitter voltage	$V_{BE} = -1,5$ V	V_{CEV}	300	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	20 28	A
Base current		$I_{B(RMS)}$ I_{BM}	4 7	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	200	−	−	V
Collector - emitter cut-off current $V_{CE} = 300$ V, $V_{BE} = -1.5$ V $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 4$ V, $I_C = 1$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 10$ A, $I_B = 1$ A	$V_{CE\ sat}$	−	−	0.9	V
Base-emitter saturation voltage $I_C = 10$ A, $I_B = 1$ A	V_{BEsat}	−	−	1.4	V

These specifications are subjet to change without notice.
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Ref.DSJBT10B20

THOMSON COMPONENTS SEMICONDUCTEURS

J BT25B20

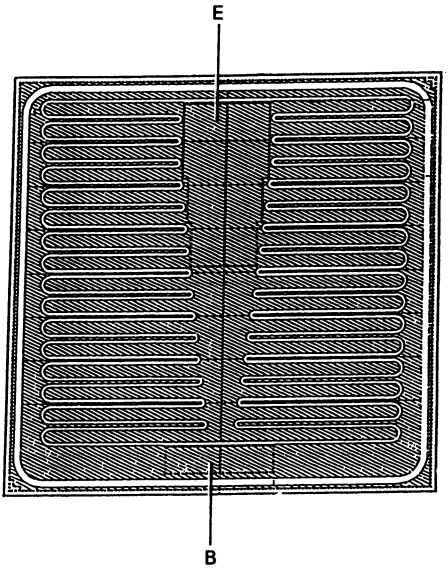
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 316
DIE SIZE	: 6.02 x 6.02mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUV61
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	200	V
Collector-emitter voltage	V_{CEV}	300	V
Emitter-base voltage	V_{EBO}	7	V
Collector current	$I_{C(RMS)}$ I_{CM}	50 75	A
Base current	$I_{B(RMS)}$ I_{BM}	8 15	A
Junction temperature	T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	200	−	−	V
Collector - emitter cut-off current V_{CE} = 250V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 5$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 12$ A, $I_B = 1.2$ A	$V_{CE\ sat}$	−	−	0.6	V
Base-emitter saturation voltage $I_C = 20$ A, $I_B = 2$ A	V_{BEsat}	−	−	1.5	V

These specifications are subjet to change without notice.
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Ref.DSJBT25B20

THOMSON
COMPONENTS
SEMICONDUCTEURS

J BT40B20

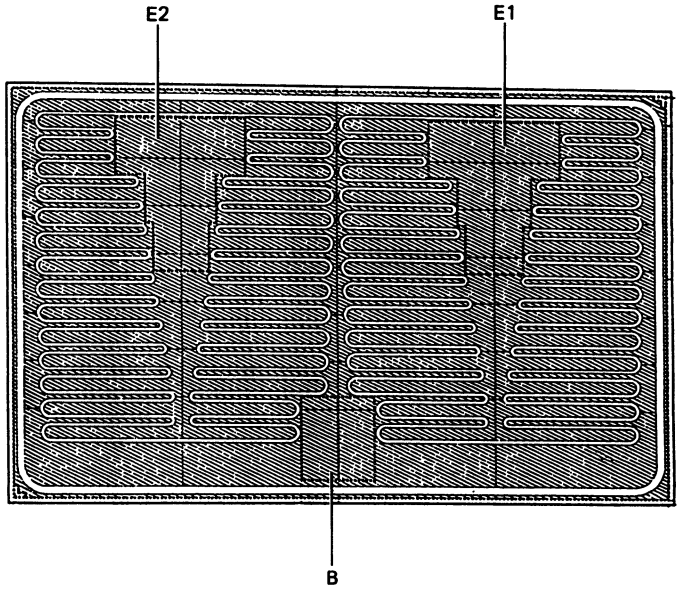
FAST SWITCHING POWER TRANSISTOR

High current, high speed transistor suited for low voltage applications.
- High current capability.
- Low saturation voltage.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 314
DIE SIZE	: 8.7 x 5.6mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUT91
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	200	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	300	V
Emitter-base voltage		V_{EBO}	10	V
Collector current		$I_{C(RMS)}$ I_{CM}	50 70	A
Base current		$I_{B(RMS)}$ I_{BM}	10 15	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	200	−	−	V
Collector - emitter cut-off current $V_{CE} = 300$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -10$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 4$ V, $I_C = 5$ A	h_{FE}	−	−	70	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 20$ A, $I_B = 1$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 20$ A, $I_B = 1$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
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Ref.DSJBT40B20

THOMSON COMPONENTS SEMICONDUCTEURS

J BT05B25

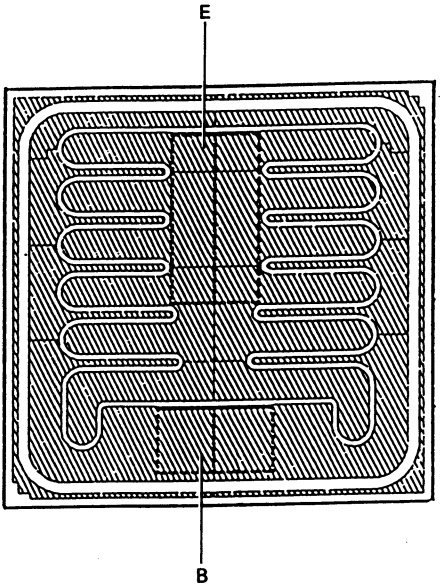
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 319
DIE SIZE	: 3.78 x 3.78mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar+ polyamide
PRODUCT ISSUE	: BUW92
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	250	V
Collector-emitter voltage	V_{CEV}	350	V
Emitter-base voltage	V_{EBO}	7	V
Collector current	$I_{C(RMS)}$ I_{CM}	12 18	A
Base current	$I_{B(RMS)}$ I_{BM}	2.5 4	A
Junction temperature	T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	250	−	−	V
Collector - emitter cut-off current $V_{CE} = 350$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1.6$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 5$ A, $I_B = 0.5$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 4$ A, $I_B = 0.4$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
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THOMSON COMPONENTS SEMICONDUCTEURS

J BT08B25

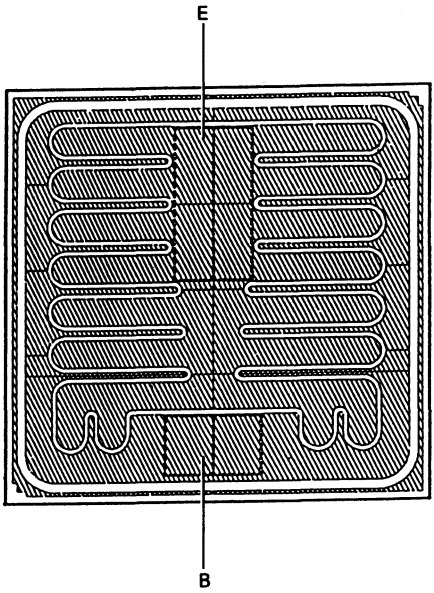
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 317
DIE SIZE	: 4.48 x 4.48mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side)
	: Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUW52
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	250	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	350	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	20 30	A
Base current		$I_{B(RMS)}$ I_{BM}	4 6	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS
$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	250	−	−	V
Collector - emitter cut-off current $V_{CE} = 350$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1.5$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 8$ A, $I_B = 0.8$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 8$ A, $I_B = 0.8$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
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Ref.DSJBT08B25

THOMSON COMPONENTS SEMICONDUCTEURS

J BT16B25

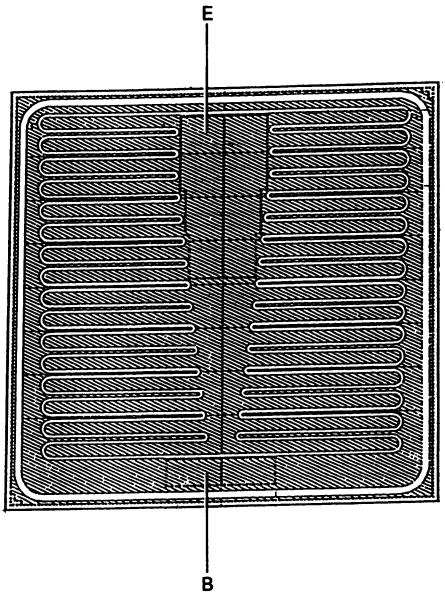
FAST SWITCHING POWER TRANSISTOR

Higher efficiency due to
- Fast switching times
- Low switching losses
- Low on-state voltage drop
- Base current requirements

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 316
DIE SIZE	: 6.02 x 6.02mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUV62
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	250	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	350	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	40 60	A
Base current		$I_{B(RMS)}$ I_{BM}	7 12	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	250	−	−	V
Collector - emitter cut-off current $V_{CE} = 300$ V, $V_{BE} = 0$ $R_{BE} =$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 5$ A	h_{FE}	−	−	60	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 16$ A, $I_B = 1.6$ A	$V_{CE\ sat}$	−	−	0.9	V
Base-emitter saturation voltage $I_C = 16$ A, $I_B = 1.6$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.DSJBT16825

THOMSON COMPONENTS SEMICONDUCTEURS

J BT35B25

FAST SWITCHING POWER TRANSISTOR

Suitable for motor-drives, S.M.P.S. converters, uninterruptible power supply operating medium low voltage supply.

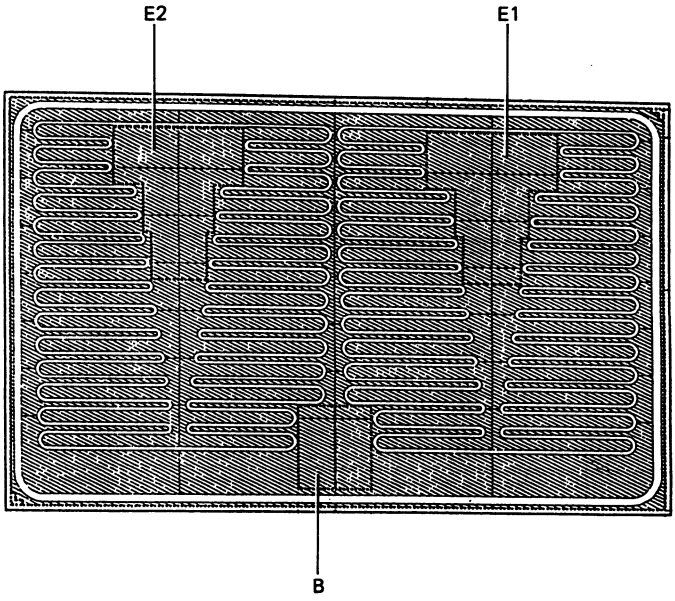
Features :

- $\beta_F > 10$ at $I_C = 35$ A.
- High efficiency switching.
- Very low saturation voltage.
- Rectangular safe operating area.
- Wide accidental overload area.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 314
DIE SIZE	: 8.7 x 5.6mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUT92
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	250	V
Collector-emitter voltage	$V_{BE} = -1,5$ V	V_{CEV}	350	V
Emitter-base voltage		V_{EBO}	7	V
Emitter current		$I_{E(RMS)}$ I_{EM}	50 75	A
Base current		$I_{B(RMS)}$ I_{BM}	10 15	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS
$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	250	−	−	V
Collector - emitter cut-off current $V_{CE} = 350$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -10$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 4$ V, $I_C = 5$ A	h_{FE}	−	−	75	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 35$ A, $I_B = 3.5$ A	$V_{CE\ sat}$	−	−	1.2	V
Base-emitter saturation voltage $I_C = 35$ A, $I_B = 3.5$ A	V_{BEsat}	−	−	1.5	V

These specifications are subjet to change without notice.
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Ref.DSJBT36B25

THOMSON COMPONENTS SEMICONDUCTEURS

J BT10B30

FAST SWITCHING POWER TRANSISTOR

- Suitable for motor drives, converters SMPS and UPS.
- Mains : Medium voltage supply.

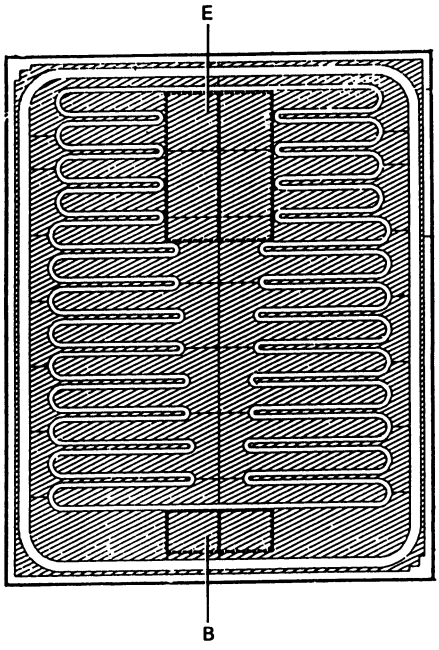
Features

-
- $\beta_F > 10$ at $I_C = 10$ A.
- High efficiency.
- Very low saturation voltage.
- Rectangular safe operating area.
- Wide accidental overload area.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 320
DIE SIZE	: 4.10 x 5.14mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar+ polyamide
PRODUCT ISSUE	: BUT62
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	300	V
Collector-emitter voltage	V_{CEV}	400	V
Emitter-base voltage	V_{EBO}	7	V
Emitter current	$I_{E(RMS)}$ I_{EM}	16 24	A
Base current	$I_{B(RMS)}$ I_{BM}	3 15	A
Junction temperature	T_j	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS:

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	300	–	–	V
Collector - base cut-off current $V_{CB} = 400$ V, $I_E = 0$	I_{CBO}	–	–	0.1	mA
Collector-emitter cut-off current $V_{CE} = 400$ V, $R_{BE} = 10\ \Omega$	I_{CER}	–	–	0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	–	–	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 1.5$ A	h_{FE}	–	–	70	–

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 10$ A, $I_B = 1$ A	$V_{CE\ sat}$	–	–	0.9	V
Base-emitter saturation voltage $I_C = 10$ A, $I_B \pm 1$ A	V_{BEsat}	–	–	1	V

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Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT10B30

THOMSON COMPONENTS SEMICONDUCTEURS

J BT30B30

FAST SWITCHING POWER TRANSISTOR

Suitable for motor drives, converters SMPS and UPS.
Mains : Low voltage supply.

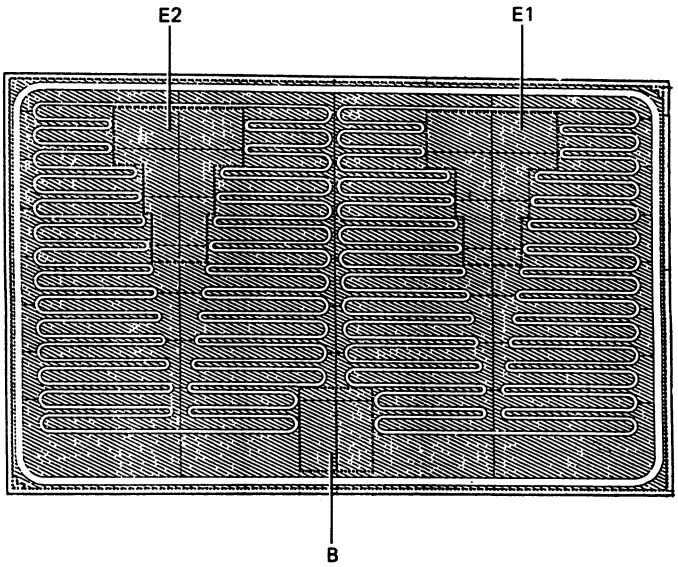
Features

- $\beta_F > 20$ at $I_C = 12$ A.
- High efficiency switching.
- Very low saturation voltage.
- Rectangular safe operating area.
- Wide accidental overload area.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 314
DIE SIZE	: 8.7 x 5.6mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Planar + polyamide
PRODUCT ISSUE	: BUT72
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	300	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	400	V
Emitter-base voltage		V_{EBO}	7	V
Emitter current		$I_{E(RMS)}$ I_{EM}	40 60	A
Base current		$I_{B(RMS)}$ I_{BM}	8 12	A
Junction temperature		T_j	− 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS
$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	300	−	−	V
Collector - base cut-off current $V_{CB} = 400$ V, $I_E = 0$	I_{CBO}	−	−	0.1	mA
Collector-emitter cut-off current $V_{CE} = 350$ V, $R_{BE} = 10\ \Omega$	I_{CER}	−	−	0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 3$ A	h_{FE}	−	−	75	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 30$ A, $I_B = 3$ A	$V_{CE\ sat}$	−	−	0.9	V
Base-emitter saturation voltage $I_C = 30$ A, $I_B = 3$ A	V_{BEsat}	−	−	1.3	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

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Ref.DSJBT30B30

THOMSON COMPONENTS SEMICONDUCTEURS

J BT02B45

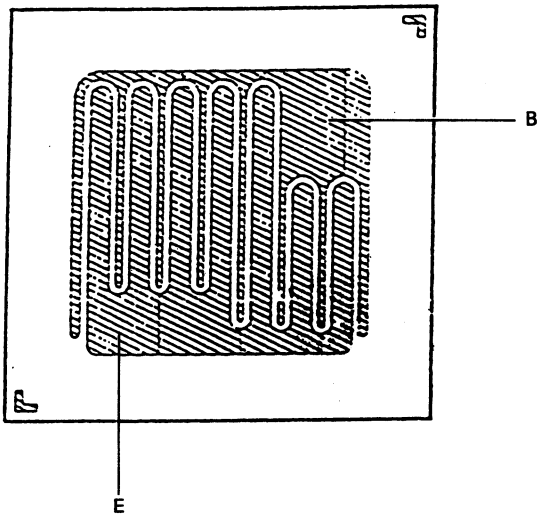
NPN HIGH VOLTAGE SWITCHING TRANSISTOR

High voltage, high speed transistor suited for :
- The 220/380 V mains.
- Switch mode power supply.
- DC/DC and DC/AC converters.
- Motor control.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 313
DIE SIZE	: 2.92 x 2.92mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: SiO_2
PRODUCT ISSUE	: BUV46
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	400	V
Collector-emitter voltage	$V_{BE} = -2.5$ V	V_{CEX}	850	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	6 8	A
Base current		$I_{B(RMS)}$ I_{BM}	2 4	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS
$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	450	−	−	V
Collector - emitter cut-off current $V_{CB} =$, $I_E = 0$	I_{CBO}	−	−	0.1	mA
Collector-emitter cut-off current $V_{CE} = 800$ V, $R_{BE} = 10\ \Omega$	I_{CER}	−	−	0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 0.5$ A	h_{FE}	−	−	40	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 1$ A, $I_B = 0.2$ A	$V_{CE\ sat}$	−	−	1	V
Base-emitter saturation voltage $I_C = 1$ A, $I_B = 0.2$ A	V_{BEsat}	−	−	1.1	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT02B45

THOMSON COMPONENTS SEMICONDUCTEURS

J BT05B45

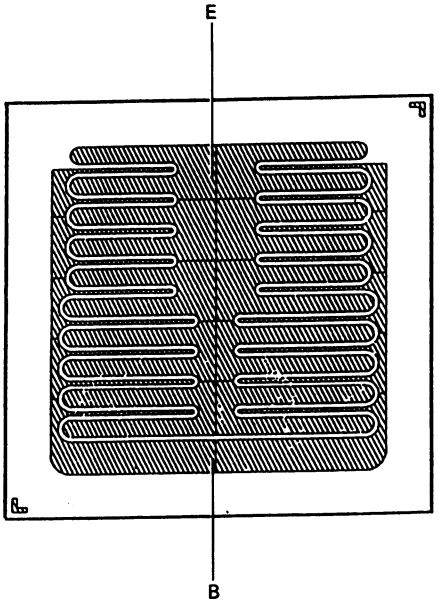
NPN HIGH VOLTAGE SWITCHING TRANSISTOR

High voltage, high speed transistor suited for :
- The 220/380 V mains.
- Switch mode power supply.
- DC/DC and DC/AC converters.
- Motor control.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 303
DIE SIZE	: 4.39 x 4.39mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: SiO_2
PRODUCT ISSUE	: BUV47
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	450	V
Collector-emitter voltage	$V_{BE} = -2.5$ V	V_{CEX}	850	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	9 15	A
Base current		$I_{B(RMS)}$ I_{BM}	3 6	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	450	−	−	V
Collector - emitter cut-off current $V_{CE} = 850$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.15 0.20	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward curren gain $V_{CE} = 5$ V, $I_C = 0.5$ A	h_{FE}	−	−	30	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 5$ A, $I_B = 1$ A	$V_{CE\ sat}$	−	−	1.5	V
Base-emitter saturation voltage $I_C = 5$ A, $I_B = 1$ A	V_{BEsat}	−	−	1.6	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT05B45

THOMSON COMPONENTS SEMICONDUCTEURS

J BT08B45

NPN HIGH VOLTAGE SWITCHING TRANSISTOR

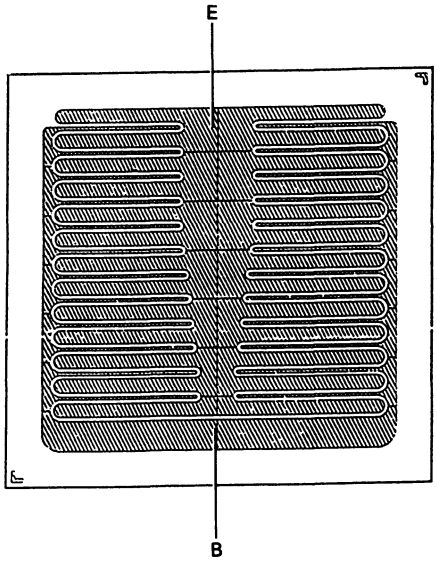
High voltage, high speed transistor suited for use on the 220 and 380 V mains.

- Suitable for switch mode power supply, UPS, DC and AC motor control.

SUPERSWITCH

SPECIFICATIONS

RACE PROCESS	: 305
DIE SIZE	: 5.4 x 5.4mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: Si O_2
PRODUCT ISSUE	: BUV48
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	450	V
Collector-emitter voltage	$V_{BE} = -2.5$ A	V_{CEV}	850	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{C(RMS)}$ I_{CM}	15 30	A
Base current		$I_{B(RMS)}$ I_{BM}	4 20	A
Junction temperature		T_j	− 65 to + 175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	450	−	−	V
Collector - emitter cut-off current $V_{CE} = 850$ V, $V_{BE} = 0$ $R_{BE} = 10\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.1 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward curren gain $V_{CE} = 5$ V, $I_C = 1.5$ A	h_{FE}	−	−	30	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 8$ A, $I_B = 1.6$ A	$V_{CE\ sat}$	−	−	1.5	V
Base-emitter saturation voltage $I_C = 10$ A, $I_B = 2$ A	V_{BEsat}	−	−	1.6	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT08845

THOMSON
COMPONENTS
SEMICONDUCTEURS

J BT12B45

FAST SWITCHING POWER TRANSISTOR

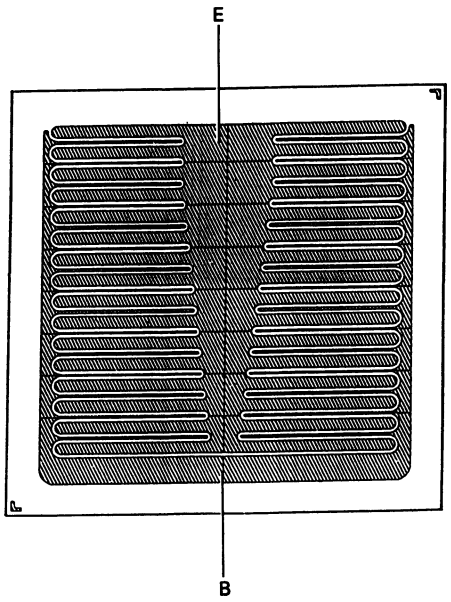
High voltage, high speed transistor suited for use on the 220 and 380 V mains.

- Suitable for switch mode power supply, UPS, DC and AC motor control.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 306
DIE SIZE	: 6.32 x 6.32mm
DIE THICKNESS	: 0.375mm ± 0.025
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: $Si O_2$
PRODUCT ISSUE	: 1/2 BUX348
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	450	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	850	V
Emitter-base voltage		V_{EBO}	7	V
Collector current		$I_{E\ (RMS)}$ I_{EM}	45 60	A
Base current		$I_{B(RMS)}$ I_{BM}	9 15	A
Junction temperature		T_j	− 65 to + 200	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	450	−	−	V
Collector - emitter cut-off current $V_{CE} = 850$ V, $V_{BE} = 0$ $R_{BE} = 5\ \Omega$	 I_{CES} I_{CER}	 − −	 − −	 0.2 0.2	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	−	−	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 2$ A	h_{FE}	−	−	35	−

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 12$ A, $I_B = 2.4$ A	$V_{CE\ sat}$	−	−	1.2	V
Base-emitter saturation voltage $I_C = 15$ A, $I_B = 3$ A	V_{BEsat}	−	−	1.5	V

These specifications are subjet to change without notice.
Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DSJBT12B45

THOMSON COMPONENTS SEMICONDUCTEURS

J BT16B45

FAST SWITCHING POWER TRANSISTOR

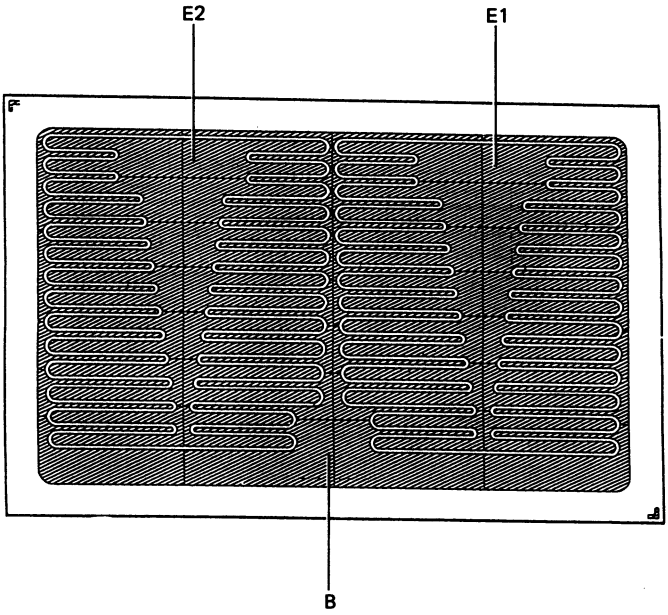
High voltage, high speed transistor suited for use on the 220 and 380 V mains.

- Suitable for switch mode power supply, UPS, DC and AC motor control.

SUPERSWITCH 2

SPECIFICATIONS

RACE PROCESS	: 304
DIE SIZE	: 9 x 5.9mm
DIE THICKNESS	: 0.4mm ± 0.05
METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: $Si O_2$
PRODUCT ISSUE	: BUX98P
QUALIFICATION LOT CASE	: TO3



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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-emitter voltage		V_{CEO}	450	V
Collector-emitter voltage	$V_{BE} = -1.5$ V	V_{CEV}	850	V
Emitter-base voltage		V_{EBO}	7	V
Emitter current		$I_{E(RMS)}$ I_{EM}	30 45	A
Base current		$I_{B(RMS)}$ I_{BM}	6 10	A
Junction temperature		T_j	– 65 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$ (unless otherwise specified)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector - emitter breakdown voltage $I_B = 0$, $I_C = 50$ mA	$V_{(BR)CEO}$	450	–	–	V
Collector - emitter cut-off current $V_{CE} = 850$ V, $V_{BE} = 0$ $R_{BE} = 5\,\Omega$	 I_{CES} I_{CER}	 – –	 – –	 0.2 0.1	mA
Emitter-base cut-off current $V_{BE} = -7$ V, $I_C = 0$	I_{EBO}	–	–	1	mA
Forward current gain $V_{CE} = 5$ V, $I_C = 3.5$ A	h_{FE}	–	–	35	–

ON CHARACTERISTICS

Collector - emitter saturation voltage $I_C = 16$ A, $I_B = 3.2$ A	$V_{CE\,sat}$	–	–	1.2	V
Base-emitter saturation voltage $I_C = 20$ A, $I_B = 4$ A	V_{BEsat}	–	–	1.5	V

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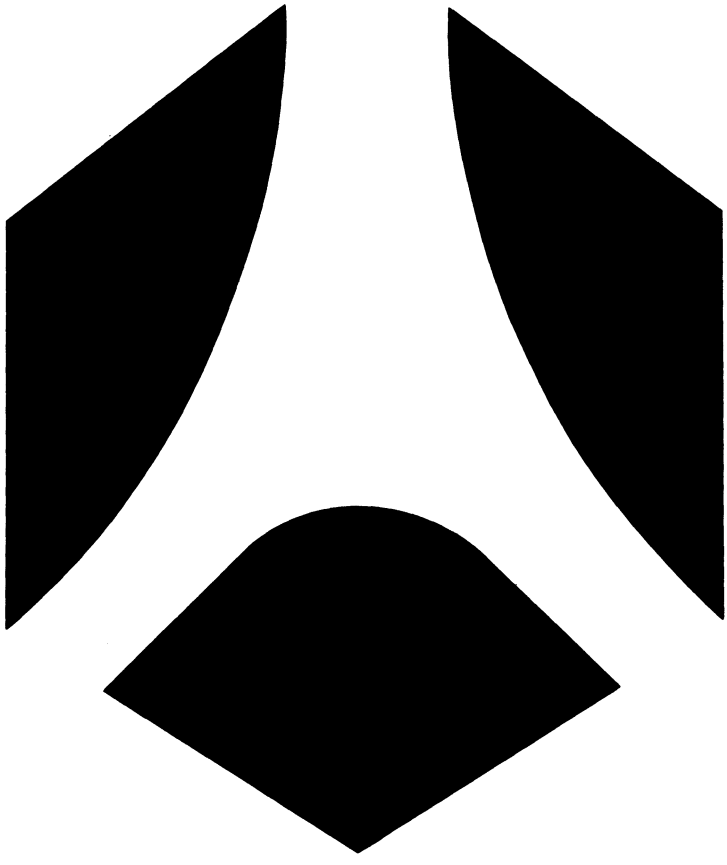
Ref.DS/BT16B45



Diodes

500 mW Zener diodes chips offering a large voltage range : 2.4 V to 62 V

ZENER

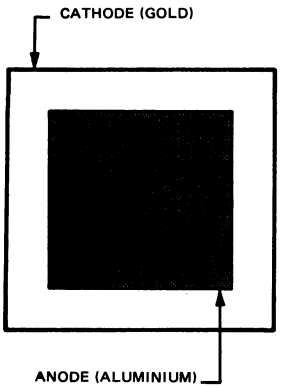
P_{tot} = 500mV

2.4 V ⩽ $V_{ZT\ nom}$ ⩽ 62 V

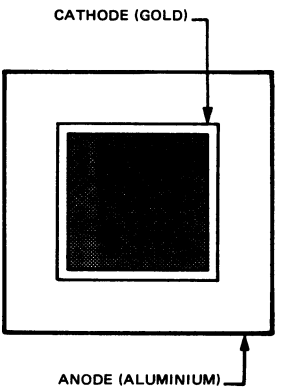
SPECIFICATIONS

METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: $Si\ O_2$
QUALIFICATION	
LOT CASE	: TO39

RACE PROCESS	: ZLBTSAL (2V4 to 3V9) : ZMBTAAL (4V3 to 5V1)
DIE SIZE	: Cathode : 0.5 x 0.5mm : Anode : 0.32 x 0.32mm
DIE THICKNESS	: 0.17mm ± 0.02



RACE PROCESS	: ZKZENAL (5V6 to 62)
DIE SIZE	: Cathode : 0.5 x 0.5mm : Anode : 0.25 x 0.25mm
DIE THICKNESS	: 0.17mm ± 0.02



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MAXIMUM RATINGS $T_{amb} = + 25°C$

Rating	Symbol	Value	Unit
DC power dissipation	P_{tot}	500	mW
Continuous reverse current	I_{ZM}	See below	mA
Non repetitive peak reverse current (sinusoidal pulse 10 ms)	I_{ZSM}	See below	mA
Operating temperature	T_{oper}	− 55 to + 175	°C
Storage temperature	T_{stg}	− 65 to + 175	°C
Maximum junction temperature	T_j	175	°C

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = + 25°C$ (unless otherwise specified)

Part number	V_{ZT}/I_{ZT} (V) min	V_{ZT}/I_{ZT} (V) max	I_{ZT} (mA)	I_R/V_R ($T_{amb} = 25°C$ (μA)	V_R (V)	I_{ZM}	I_{ZSM}
J BZX 55 C 2V4	2.28	2.56	5	50	1	155	1720
J BZX 55 C 2V7	2.5	2.9	5	10	1	135	1600
J BZX 55 C 3V9	2.8	3.2	5	4	1	125	1500
J BZX 55 C 3V3	3.1	3.5	5	2	1	115	1400
J BZX 55 C 3V6	3.4	3.8	5	2	1	105	1330
J BZX 55 C 3V9	3.7	4.1	5	2	1	95	1270
J BZX 55 C 4V3	4.0	4.6	5	1	1	90	1220
J BZX 55 C 4V7	4.4	5.0	5	0,5	1	85	1160
J BZX 55 C 5V1	4.8	5.4	5	0,1	1	80	1100
J BZX 55 C 5V6	5.2	6.0	5	0,1	1	70	1040
J BZX 55 C 6V2	5.8	6.6	5	0,1	2	64	980
J BZX 55 C 6V8	6.4	7.2	5	0,1	3	58	900
J BZX 55 C 7V5	7,0	7,9	5	0,1	5	53	810
J BZX 55 C 8V2	7,7	8,7	5	0,1	6,2	47	760
J BZX 55 C 9V1	8,5	9,6	5	0,1	6,8	43	670
J BZX 55 C 10	9.4	10.6	5	0,1	7,5	40	600
J BZX 55 C 11	10.4	11.6	5	0,1	8,2	36	550
J BZX 55 C 12	11.4	12.7	5	0,1	9,1	32	500
J BZX 55 C 13	12.4	14.1	5	0,1	10	29	450
J BZX 55 C 15	13.8	15.6	5	0,1	11	27	380
J BZX 55 C 16	15.3	17.1	5	0,1	12	24	350
J BZX 55 C 18	16.8	19.1	5	0,1	13	21	300
J BZX 55 C 20	18.8	21.2	5	0,1	15	20	270
J BZX 55 C 22	20.8	23.3	5	0,1	16	18	250
J BZX 55 C 24	22.8	25.6	5	0,1	18	16	225
J BZX 55 C 27	25.1	28.9	5	0,1	20	14	200
J BZX 55 C 30	28	32	5	0,1	22	13	190
J BZX 55 C 33	31	35	5	0,1	24	12	175
J BZX 55 C 36	34	38	5	0,1	27	11	160
J BZX 55 C 39	37	41	2.5	0,1	30	10	148
J BZX 55 C 43	40	46	2.5	0,1	33	9.2	135
J BZX 55 C 47	44	50	2.5	0,1	36	8.5	123
J BZX 55 C 51	48	54	2.5	0,1	39	7.8	113
J BZX 55 C 56	52	60	2.5	0,1	43	7.0	104
J BZX 55 C 62	58	66	2.5	0,1	47	6.4	93

$T_p \leq 50$ ms - $\sigma \leq 2$ %

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Please inquire with our sales offices about the availability of the different products.

Printed in France

Ref.DS.JBZX55C

THOMSON COMPONENTS SEMICONDUCTEURS

J BZX85C

ZENER DIODES 1.3 W

1.3 W Zener diodes chips offering a large voltage range . 2.7 V to 62 V

ZENER

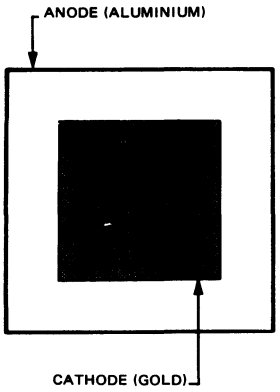
$P_{tot} = 1.3mV$

$2.7\ V \leqslant V_{ZT\ nom} \leqslant 62\ V$

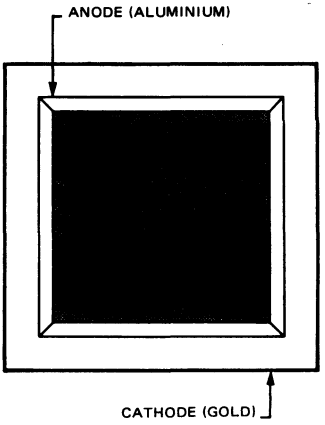
SPECIFICATIONS

METALLIZATION	: Al (front side) : Au (back side)
PASSIVATION	: $Si\ O_2$
QUALIFICATION	
LOT CASE	: TO39

RACE PROCESS	: ZLBTSAL (2V7 to 4V3) : ZMBTAAL (4V7 to 5V1)
DIE SIZE	: Cathode : 0.5 x 0.5mm : Anode : 0.32 x 0.32mm
DIE THICKNESS	: 0.17 x 0.17mm



RACE PROCESS	: ZKZENAL (5V6 to 62)
DIE SIZE	: Cathode : 0.65 x 0.65mm : Anode : 0.425 x 0.425mm
DIE THICKNESS	: 0.17mm ± 0.02



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ELECTRICAL OPERATING CHARACTERISTICS

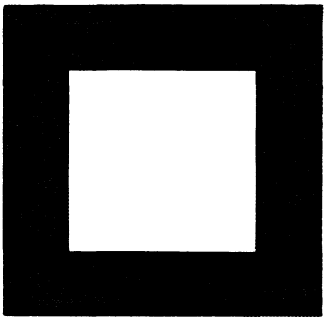
T_{amb} = + 25°C (unless otherwise specified)

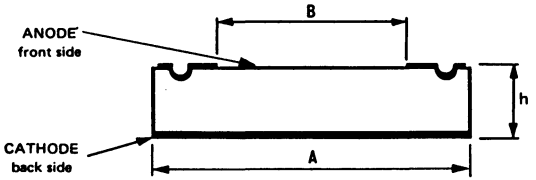
Part number	V_{RM} max (V) (1)	I_F max (mA) (1)	I_{FSM} max at t_p (s) (A) (1)	I_{FRM} max at t_p (s) (A) (1)	V_F max. at I_F (mA) (V)	I_R max. at V_R (V) (nA)	C max. at V_R (V) (pF) (2)	Storage temp. range °C (1)	Junction temp. °C (1)	Product issue Glass case DO 35-DO 41
J BAT19	10	30	0,06 at 1	–	0.4 at 1	100 at 5	1.2 at 0	–65 to +150	–65 to +125	BAT 19 BAT 29 BAR 19
J BAR10	20	35	0.1 at 1	–	0.41 at 1	100 at 15	1.2 at 0	–65 to +200	–65 to +200	BAR 10 1N 5712 BAR 11
J BAR28	70	15	0.05 at 1	–	0.41 at 1	200 at 50	2 at 0	–65 to +200	–65 to +200	BAR 28 1N 5711 1N 6263
J BAT42	30	200	4 at 0.01	0.5 at 1	0.4 at 10	500 at 25	7 typ at 1	–65 to +150	–65 to +125	BAT 42/43
J BAT48	40	350	1.5 at 1	1 at 1	0.4/10 -0.9/100	2000 at 10	12 typ at 1	–65 to +150	–65 to +125	BAT 47/48
J BAT41	100	100	0.75 at 0.01	0.35 at 1	0.45 at 1	100 at 50	2 typ at 1	–65 to +150	–65 to +125	BAT 41
J BAT46	100	150	0.75 at 0.01	0.35 at 1	0.45 at 10	2000 at 50	6 typ at 1	–65 to +150	–65 to +125	BAT 46
J BYV10-20A	20	–	25 at 0.01	–	0.45 at 1000	300 µA at 20	330 typ at 0	–65 to + 150	–65 to +125	BYV 10-20 A
J BYV10-40	40	–	25 at 0.01	–	0.055 at 1000	500 µA at 40	200 typ at 0	–65 to +150	–65 to +125	BYV 10-20 BYV 10-30 BYV 10-40
J BYV10-60	60	–	20 at 0.01	–	0.7 at 1000	500 µA at 60	150 typ at 0	–65 to +150	–65 to +125	BYV 10-60
J BAT49	80	–	10 at 0.01	3 at 1	0.42 at 100	200 µA at 80	120 typ at 0	–65 to +150	–65 to +125	BAT 49

(1) : Maximum ratings

(2) : Tested in package DO35 - DO41

Part number	Dimensions A (mm)	V_{RRM} (V)	Anode Dimensions B (mm)	Die Thickness h (mm)	Race Process	Metallization		Passivation
						Front side	Back side	
2 A								
J R2-40 J R2-60 J R2-80 J R2-100	1.5 x 1.5 ± 0.1	400 600 800 1000	0.7 x 0.7 ± 0.1	0.3 ± 0.01	A15R	Al	Sublayer + Au	Si O2
6 A								
J R6-40 J R6-60 J R6-80 J R6-100	2.8 x 2.8 ± 0.1	400 600 800 1000	1.8 x 1.8 ± 0.1	0.3 ± 0.01	A28R	Al	Sublayer + Au	Si O2
12 A								
J R12-40 J R12-60 J R12-80 J R12-100	3.8 x 3.8 ± 0.1	400 600 800 1000	2.7 x 2.7 ± 0.1	0.3 ± 0.01	A38R	Ni-Au	Ni-Au	Si O2
40 A								
J R40-40 J R40-60 J R40-80 J R40-100	5.3 x 5.3 ± 0.1	400 600 800 1000	4.2 x 4.2 ± 0.1	0.3 ± 0.01	A53R	Ni-Au	Ni-Au	Si O2





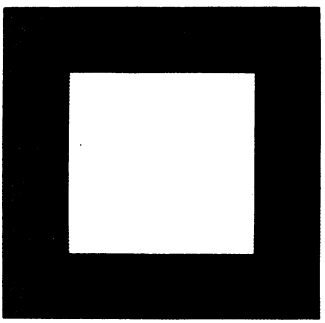
ELECTRICAL OPERATING CHARACTERISTICS

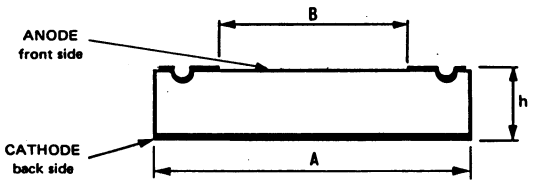
T_{amb} = + 25°C (unless otherwise specified)

Part number	I_O (A)	V_{RRM} (V)	I_{FSM} 10 ms (A) (1)	VF / IF max (V)	(A)	I_R/V_{RRM} max (µA)	t_{rr} ▲ max. (ns)	Product issues
2 A								
J R2-40	2	400	40	1.2	2	10	–	
J R2-60		600	40	1.2				
J R2-80		800	30	1.4				
J R2-100		1000	30	1.4				
6 A								
J R6-40	6	400	100	1.4	18 (2)	20		BY 239
J R6-60		600	100	1.4				
J R6-80		800	80	1.6				
J R6-100		1000	80	1.6				
12 A								
J R12-40	12	400	200	1.4	35 (2)	20	–	BYW 88
J R12-60		600	200	1.4				
J R12-80		800	160	1.6				
J R12-100		1000	160	1.6				
40 A								
J R40-40	40	400	800	1.4	120 (2)	50	–	1 N 3768
J R40-60		600	800	1.4				
J R40-80		800	640	1.6				
J R40-100		1000	640	1.6				

(1) : Maximum ratings
(2) : Tested by sampling

Part number	Dimensions A (mm)	V_{RRM} (V)	Anode Dimensions B (mm)	Die Thickness h (mm)	Race Process	Metallization		Passivation
						Front side	Back side	
1.5 A								
J RFV1.5-05 J RFV1.5-10 J RFV1.5-15 J RFV1.5-20	1.5 x 1.5 ± 0.1	50 100 150 200	0.7 x 0.7 ± 0.1	0.3 ± 0.01	A15V	Ni-Au	Ni-Au	Si O2
3 A								
J RFV3-05 J RFV3-10 J RFV3-15 J RFV3-20	1.8 x 1.8 ± 0.1	50 100 150 200	1 x 1 ± 0.1	0.3 ± 0.01	A18V	Ni-Au	Ni-Au	Si O2
7 A								
J RFV7-05 J RFV7-10 J RFV7-15 J RFV7-20	2.5 x 2.5 ± 0.1	50 100 150 200	1.6 x 1.6 ± 0.1	0.3 ± 0.01	A25V	Al	Sublayer + Au	Si O2
12 A								
J RFV12-05 J RFV12-10 J RFV12-15 J RFV12-20	3 x 3 ± 0.1	50 100 150 200	2 x 2 ± 0.1	0.3 ± 0.01	A30V	Ni - Au or Al	Ni - Au or Sublayer + Au	Si O2
20 A								
J RFV20-05 J RFV20-10 J RFV20-15 J RFV20-20	4.3 x 4.3 ± 0.1	50 100 150 200	3.2 x 3.2 ± 0.1	0.3 ± 0.01	A43V	Ni - Au or Al	Ni - Au or Sublayer + Au	Si O2
50 A								
J RFV50-05 J RFV50-10 J RFV50-15 J RFV50-20	6.3 x 6.3 ± 0.1	50 100 150 200	5.2 x 5.2 ± 0.1	0.3 ± 0.01	A63V	Ni - Au or Al	Ni - Au or Sublayer + Au	Si O2





ELECTRICAL OPERATING CHARACTERISTICS

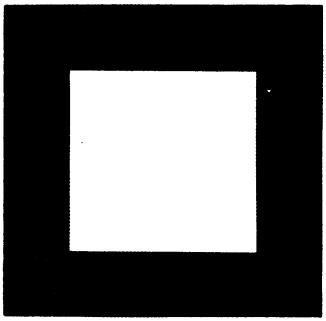
$T_{amb} = +25°C$ (unless otherwise specified)

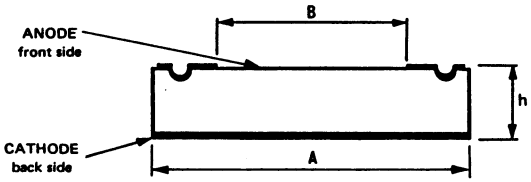
Part number	I_O (A)	V_{RRM} (V)	I_{FSM} (A) (1)	V_F max (V)	I_F (A)	I_R/V_{RRM} max (μA)	t_{rr} ▲ max. (ns)	Product issues
1,5 A								
J RFV1.5-05 J RFV1.5-10 J RFV1.5-15 J RFV1.5-20	1.5	50 100 150 200	50	0.95	1.5	10	35	BYW 100
3 A								
J RFV3-05 J RFV3-10 J RFV3-15 J RFV3-20	3	50 100 150 200	70	0.95	3	10	35	BYW 98
7 A								
J RFV7-05 J RFV7-10 J RFV7-15 J RFV7-20	7	50 100 150 200	100	0.95	7 (2)	20	35	BYW 80
12 A								
J RFV12-05 J RFV12-10 J RFV12-15 J RFV12-20	12	50 100 150 200	200	0.95	12 (2)	30	35	BYW 81
20 A								
J RFV20-05 J RFV20-10 J RFV20-15 J RFV20-20	20	50 100 150 200	500	0.95	20 (2)	50	50	BYW 77
50 A								
J RFV50-05 J RFV50-10 J RFV50-15 J RFV50-20	50	50 100 150 200	1500	0.95	50 (2)	100	60	BYW 78

▲ t_{rr} test conditions : $I_F = 1$ A $V_R = -30$ V dip/dt $= -50$ A/μs

(1) : Maximum ratings
(2) : Tested by sampling

Part number	Dimensions A (mm)	V_{RRM} (V)	Anode Dimensions B (mm)	Die Thickness h (mm)	Race Process	Metallization		Passivation
						Front side	Back side	
1 A								
J BYT01-20 J BYT01-30 J BYT01-40	1.5 x 1.5 ± 0.1	200 300 400	0.7 x 0.7 ± 0.1	0.3 ± 0.01	A15W	Ni - Au	Ni - Au	Si O2
3 A								
J BYT03-20 J BYT03-30 J BYT03-40	1.8 x 1.8 ± 0.1	200 300 400	1 x 1 ± 0.1	0.3 ± 0.01	A18W	Ni - Au	Ni - Au	Si O2
8 A								
J BYT08-20 J BYT08-30 J BYT08-40	2.8 x 2.8 ± 0.1	200 300 400	1.8 x 1.8 ± 0.1	0.3 ± 0.01	A28W	Al	Sublayer Au	Si O2
12 A								
J BYT12-20 J BYT12-30 J BYT12-40	3.3 x 3.3 ± 0.1	200 300 400	2.2 x 2.2 ± 0.1	0.3 ± 0.01	A33W	Ni - Au	Ni - Au	Si O2
30 A								
J BYT30-20 J BYT30-30 J BYT30-40	3.3 x 4.3 ± 0.1	200 300 400	3.2 x 3.2 ± 0.1	0.3 ± 0.01	A43W	Ni - Au Al	Ni - Au or Sublayer + Au	Si O2
60 A								
J BYT60-20 J BYT60-30 J BYT60-40	6.3 x 6.3 ± 0.1	200 300 400	5.2 x 5.2 ± 0.1	0.3 ± 0.01	A63W	Ni - Au Al	Ni - Au or Sublayer + Au	Si O2





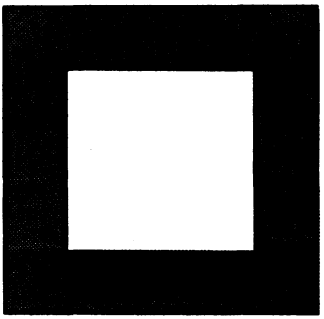
ELECTRICAL OPERATING CHARACTERISTICS

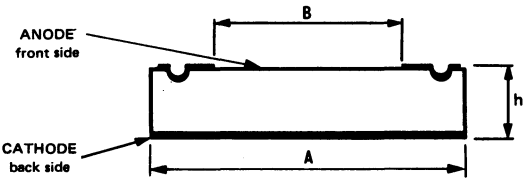
T_{amb} = + 25°C (unless otherwise specified)

Part number	I_O (A)	V_{RRM} (V)	I_{FSM} 10 ms (A) (1)	V_F @ $I_F = I_O$ max (V)	I_R/V_{RRM} max (μA)	t_{rr} ▲ max (ns)	Product issues
1 A							
J BYT01-20 J BYT01-30 J BYT01-40	1	200 300 400	30	1.5	10	25	BYT 01
3 A							
J BYT03-20 J BYT03-30 J BYT03-40	3	200 300 400	50	1.5	10	25	BYT 03
8 A							
J BYT08-20 J BYT08-30 J BYT08-40	8	200 300 400	100	1.5 (2)	15	35	BYT 08
12 A							
J BYT12-20 J BYT12-30 J BYT12-40	12	200 300 400	200	1.5 (2)	15	50	BYT 12
30 A							
J BYT30-20 J BYT30-30 J BYT30-40	30	200 300 400	500	1.5 (2)	35	50	BYT 30
60 A							
J BYT60-20 J BYT60-30 J BYT60-40	60	200 300 400	800	1.5 (2)	60	50	BYT 60

▲ t_{rr} test conditions $I_F = 0.5$ A $I_R = 1$ A $I_{rr} = 0.25$ A

Part number	Dimensions A (mm)	V_{RRM} (V)	Anode Dimensions B (mm)	Die Thickness h (mm)	Race Process	Metallization		Passivation
						Front side	Back side	
2 A								
J RF2-20 J RF2-40 J RF2-60	1.5 x 1.5 ± 0.1	200 400 600	0.7 x 0.7 ± 0.1	0.3 ± 0.01	A15B	Ni - Au Al	Ni - Au Au + Sublayer	Si O2
8 A								
J RF8-20 J RF8-40 J RF8-60	2.8 x 2.8 ± 0.1	200 400 600	1.8 x 1.8 ± 0.1	0.3 ± 0.01	A28B	Ni - Au Al	Ni - Au Au + Sublayer	Si O2
12 A								
J RF12-20 J RF12-40 J RF12-60	3.3 x 3.3 ± 0.1	200 400 600	2.2 x 2.2 ± 0.1	0.3 ± 0.01	A33B	Ni - Au	Ni - Au	Si O2
20 A								
J RF20-20 J RF20-40 J RF20-60	4.3 x 4.3 ± 0.1	200 400 600	3.2 x 3.2 ± 0.1	0.3 ± 0.01	A43B	Ni - Au	Ni - Au	Si O2
30 A								
J RF30-20 J RF30-40 J RF30-60	4.8 x 4.8 ± 0.1	200 400 600	3.7 x 3.7 ± 0.1	0.3 ± 0.01	A48B	Ni - Au	Ni - Au	Si O2
60 A								
J RF60-20 J RF60-40 J RF60-60	6.3 x 6.3 ± 0.1	200 400 600	5.2 x 5.2 ± 0.1	0.3 ± 0.01	A63B	Ni - Au	Ni - Au	Si O2





ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C (unless otherwise specified)

Part number	I_O (A)	V_{RRM} (V)	I_{FSM} 10 ms (A) (1)	V_F @ $I_F = I_O$ max (V)	I_R/V_{RRM} max (μA)	t_{rr}▲ max (ns)	Product issues
2 A							
J RF2-20 J RF2-40 J RF2-60	2	200 400 600	50	1.6	10	200	
8 A							
J RF8-20 J RF8-40 J RF8-60	8	200 400 600	100	1.4	20	200	
12 A							
J RF12-20 J RF12-40 J RF12-60	12	200 400 600	150	1.4 (2)	25	200	1N 3891 1N 3893 BYX 62-600
20 A							
J RF20-20 J RF20-40 J RF20-60	20	200 400 600	225	1.4 (2)	50	200	1N 3901 1N 3903 BYX 63-600
30 A							
J RF30-20 J RF30-40 J RF30-60	30	200 400 600	300	1.4 (2)	50	200	1N 3911 1N 3913 BYX 64-600
60 A							
J RF60-20 J RF60-40 J RF60-60	60	200 400 600	800	1.4 (2)	100	200	ESM 244-200 ESM 244-400 ESM 244-600

▲t_{rr} test conditions : $I_F = 1$ A $V_R = 30$ V dip/dt = 15 A/μS.

(1) : Maximum ratings
(2) : Tested by sampling

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Tel. 78.66.00.66 Telex : 375187

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Telefax. (43 222) 86.32.11-200

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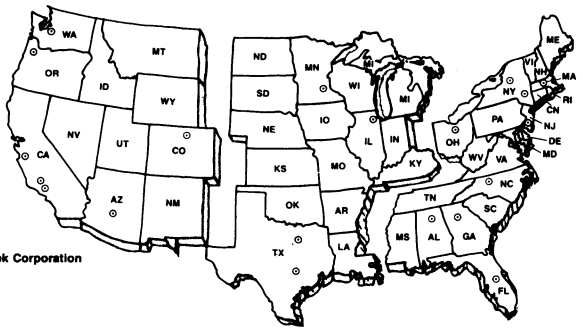

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FAX 215/362-1293

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